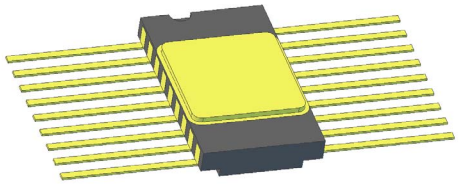
RHFLVDSR2D2

Rad-hard dual LVDS driver-receiver

Datasheet - production data



Ceramic Flat-18

The upper metallic lid is electrically connected to ground

Features

- Dual drivers, TTL compatible inputs/LVDS outputs
- Dual receivers, LVDS inputs/TTL compatible outputs
- Individual Enable/Disable function with high-impedance
- ANSI TIA/EIA-644 compliant
- 400 Mbps (200 MHz)
- Cold spare on all pins
- Fail-safe function
- 3.3 V operating power supply
- 4.8 V absolute rating
- Power consumption: 50 mW at 3.3 V
- Hermetic package
- Large input common mode: -4 V to +5 V
- Guaranteed up to 300 krad TID
- SEL immune up to 135 MeV.cm²/mg
- SET/SEU immune up to 32 MeV.cm²/mg

Description

Dual low voltage differential signaling (LVDS), driver receiver designed, packaged and qualified for use in aerospace environments in a low-power and fast-transmission standard, and operating at 3.3 V power supply (3.6 V max operating and 4.8 V AMR). The RHFLVDSR2D2 operates over a controlled impedance of 100-ohm transmission media that may be printed circuit board traces, back planes, or cables.

The circuit features an internal fail-safe function to ensure a known state in case of an input short circuit or floating input. All pins have cold spare buffers to ensure they are in high impedance when V_{CC} is tied to GND.

The RHFLVDSR2D2 can operate over a large temperature range of -55 °C to +125 °C and it is housed in an hermetic Ceramic Flat-18 package.

Table 1. Device summary

Reference	SMD pin	Quality level	Package	Lead finish	Mass	EPPL[1]	Temp. range
RHFLVDSR2D2K1	-	Engineering model	Ceramic Flat-18	Gold	-	-	-55 °C to 125 °C
RHFLVDSR2D2K01V[2]	TBD	QML-V flight				Target	

1. EPPL = ESA preferred part list
2. Not yet in full production

Contents

1 Functional description and pin configuration

Figure 1. Functional diagram and pinout

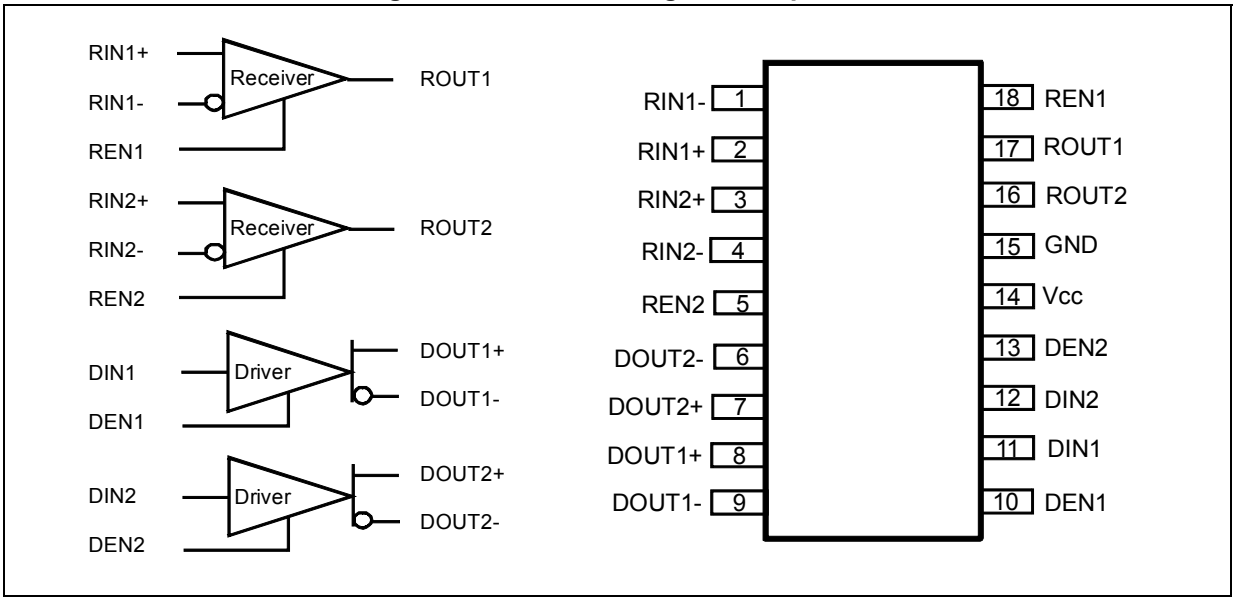


Table 2. Truth table: Driver

Enables	Input	Output	
DEN	**DIN**	**DOUT+**	**DOUT-**
L	X	Z	Z
H or floating (internal pull-up)	L	L	H
	H	H	L
	Open	L	H

Table 3. Truth table: Receiver

Enables	Input	Output
REN	**RIN+ - RIN-**	**ROUT**
L	X	Z
H or floating (internal pull-up)	Vid ≥ 0.1 V	H
	Vid ≤ -0.1 V	L
	-0.1 V < Vid < +0.1 V	?
	Full fail-safe Open/Short or terminated	H

Note: Vid = (VIN+) - (VIN-), *L = low level, H = high Level, X = don't care, Z = high impedance (off)*

2 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	4.8	V
V_i	TTL inputs (operating or cold-spare)	-0.3 to 4.8	
V_{CM}	LVDS common mode (operating or cold-spare)	-5 to +6	
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximun junction temperature	+150	
R_{thjc}	Thermal resistance junction to case(2)	21	°C/W
ESD	HBM: Human body model – All pins excepted LVDS inputs and outputs – LVDS inputs and outputs vs. GND	 2 8	kV
	CDM: Charge device model	500	V

1. All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.
2. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

Table 5. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CM}	Static common mode on the receiver	- 4		+ 5	
V_{IN}	Driver DC input voltage (TTL inputs)	0		3.6	
T_A	Ambient temperature range	-55		+125	°C
CL	TTL output capacitive load of the receiver	3			pF

3 Electrical characteristics

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDSR2D2 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in *Table 7: Electrical characteristics* apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiations

Type	Characteristics	Value	Unit
TID	High-dose rate (50 - 300 rad/sec)	300	krad
Heavy ions	SEL immunity up to: (with a particle angle of 60 °, at 125 °C)	135	MeV.cm²/mg
	SEL immunity up to: (with a particle angle of 0 °, at 125 °C)	67	
	SET/SEU immunity up to: (at 25 °C)	32	

In *Table 7* below, V_{CC} = 3 V to 3.6 V, capa-load (CL) = 10 pF, typical values are at T_{amb} = +25 °C, min. and max values are at T_{amb} = - 55 °C and + 125 °C unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Whole circuit						
I_{CC}	Total enabled supply current, drivers and receivers enabled, not switching	Driver: V_{IN} = 0 V or V_{CC} and load = 100 Ω receiver: V_{ID} = 400 mV		15	19	mA
I_{CCZ}	Total disabled supply current, loaded or not loaded, drivers and receivers disabled	R_{EN} and D_{EN} = GND Driver: V_{IN} = 0 V or V_{CC} Receiver: V_{ID} = 400 mV			4	
V_{IH}	Input voltage high	R_{EN}, D_{EN}, and TTL inputs	2		V_{CC}	V
V_{IL}	Input voltage low		GND		0.8	
I_{IH}	High level input current	R_{EN}, D_{EN}, and TTL inputs V_{CC} = 3.6 V, V_{IN} = V_{CC}	-10		10	µA
I_{IL}	Low level input current	R_{EN}, D_{EN} and TTL inputs V_{CC} = 3.6 V, V_{IN} = 0	-10		10	
I_{OFF} (1)	LVDS outputs power off leakage current	V_{CC} = 0 V, V_{OUT} = 3.6 V	-50		+50	
	LVDS inputs power off leakage current	V_{CC} = 0 V, V_{IN} = -4 V to 5 V	-60		60	
	TTL I/Os power off leakage current	V_{CC} = 0 V V_{IN}, R_{EN}, and D_{EN} = 3.6 V V_{OUT} = 3.6 V	-10		10	
Driver						
V_{OH}	Output voltage high	R_L = 100 Ω			1.65	V
V_{OL}	Output voltage low		0.925			
V_{OD}	Differential output voltage		250		400	mV
DV_{OD}	Change of magnitude of V_{OD1} for complementary output states				10	
V_{OS}	Offset voltage		1.125		1.45	V
DV_{OS}	Change of magnitude of V_{OS} for complementary output states				15	mV
I_{OS}	Output short-circuit current	V_{IN}= 0V and V_{OUT-} = 0 V or V_{IN} = V_{CC} and V_{OUT+} = 0 V	-9			mA
I_{OZ}	High impedance output current	Disabled, V_{OUT} = 3.6 V or GND	-10		10	µA
C_{IN}	Input capacitance			3		pF

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PHLD}	Propagation delay time, high to low output	Load: refer to *Figure 3*	0.5		1.5	ns
t_{PLHD}	Propagation delay time, low to high output		0.5		1.5	
t_r	Differential output signal rise time			0.8		
t_f	Differential output signal fall time			0.8		
t_{SK1}	Channel-to-channel skew(2)				0.28	
t_{SK2}	Chip-to-chip skew(3)(4)				0.7	
t_{SKD}	Differential skew(5) (t_{PHLD}-t_{PLHD})				0.3	
t_{PHZ}	Propagation delay time, high level to high impedance output	Load: refer to *Figure 4*			2.8	
t_{PLZ}	Propagation delay time, low level to high impedance output				2.8	
t_{PZH}	Propagation delay time, high impedance to high level output				2.5	
t_{PZL}	Propagation delay time, high impedance to low level output				2.5	
Receiver						
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V			-100	mV
		-4 V < V_{CM} < +5 V			-130	
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V	+100			
		-4 V < V_{CM} < +5 V	+130			
V_{CMR}	Common mode voltage range	V_{ID} = 200 mVp-p	- 4		+5	V
V_{CMREJ}	Common mode rejection(6)	F = 10 MHz			300	mVp-p
I_{ID}	Differential Input current	V_{ID} = 400 mVp-p	-10		10	µA
I_{ICM}	Common mode Input current	V_{IC} = - 4 V to + 5 V	-70		70	
V_{OH}	Output voltage high	I_{OH} = -0.4 mA, V_{CC} = 3 V	2.7			V
V_{OL}	Output voltage low	I_{OL} = 2 mA, V_{CC} = 3 V			0.25	
I_{OS}	Output short circuit current	V_{OUT} = 0 V	-90		-30	mA
I_{OZ}	Output tri-state current	Disabled, V_{OUT} = 0 V or V_{CC}	-10		10	µA
C_{IN}	Input capacitance	IN+ or IN- to GND		3		pF
R_{out}	Output resistance			45		Ω
t_{PHLD}	Propagation delay time, high to low output	V_{ID} = 200 mVp-p, input pulse from 1.1 V to 1.3 V, V_{CM} = 1.2 V Load: refer to *Figure 6*	1		2.5	ns
t_{PLHD}	Propagation delay time, low to high output		1		2.5	

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SK1}	Channel-to-channel skew(2)	V_{ID} = 200 mVp-p Load: refer to *Figure 3*			0.2	ns
t_{SK2}	Chip-to-chip skew(3)(4)				0.7	
t_{SKD}	Differential skew(5) (t_{PHLD}-t_{PLHD})				0.3	
t_r	Output signal rise time	Load: refer to *Figure 3*		0.9		
t_f	Output signal fall time			0.9		
t_{PLZ}	Propagation delay time, low level to high impedance output	Load: refer to *Figure 4*			3.8	
t_{PHZ}	Propagation delay time, high level to high impedance output				3.8	
t_{PZH}	Propagation delay time, high impedance to high level output				3.8	
t_{PZL}	Propagation delay time, high impedance to low level output				3.8	
t_{D1}	Fail-safe to active time			1		µs
t_{D2}	Active to fail-safe time			1		

1. All pins except pin under test and V_{CC} are floating
2. t_{SK1} is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).
3. t_{SK2} is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.
4. Guaranteed by design
5. t_{SKD} is the maximum delay time difference between t_{PHLD} and t_{PLHD}, see *Figure 3*.
6. Guaranteed by characterization on bench.

Cold sparing

The RHFLVDSR2D2 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and V_{CC}. ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. For the drivers: in case of an LVDS input short circuit or floating inputs, the TTL outputs remain in stable logic-high state.

4 Test circuit for the driver

Figure 2. Voltage and current definition

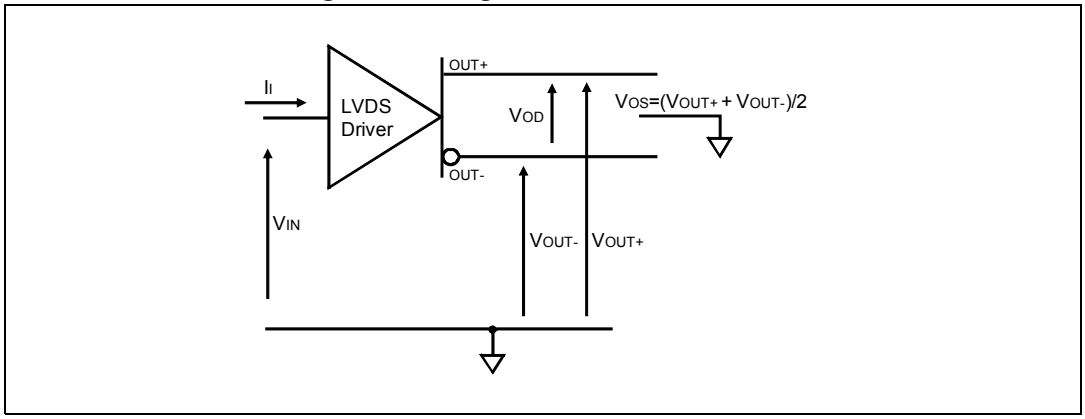
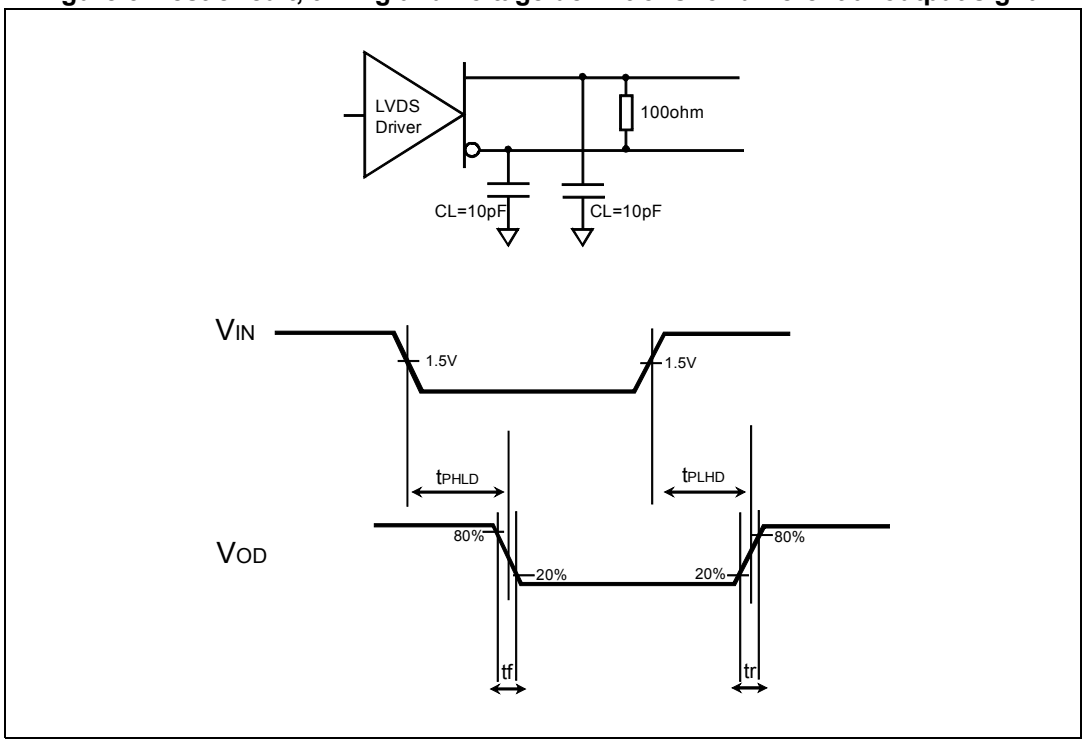
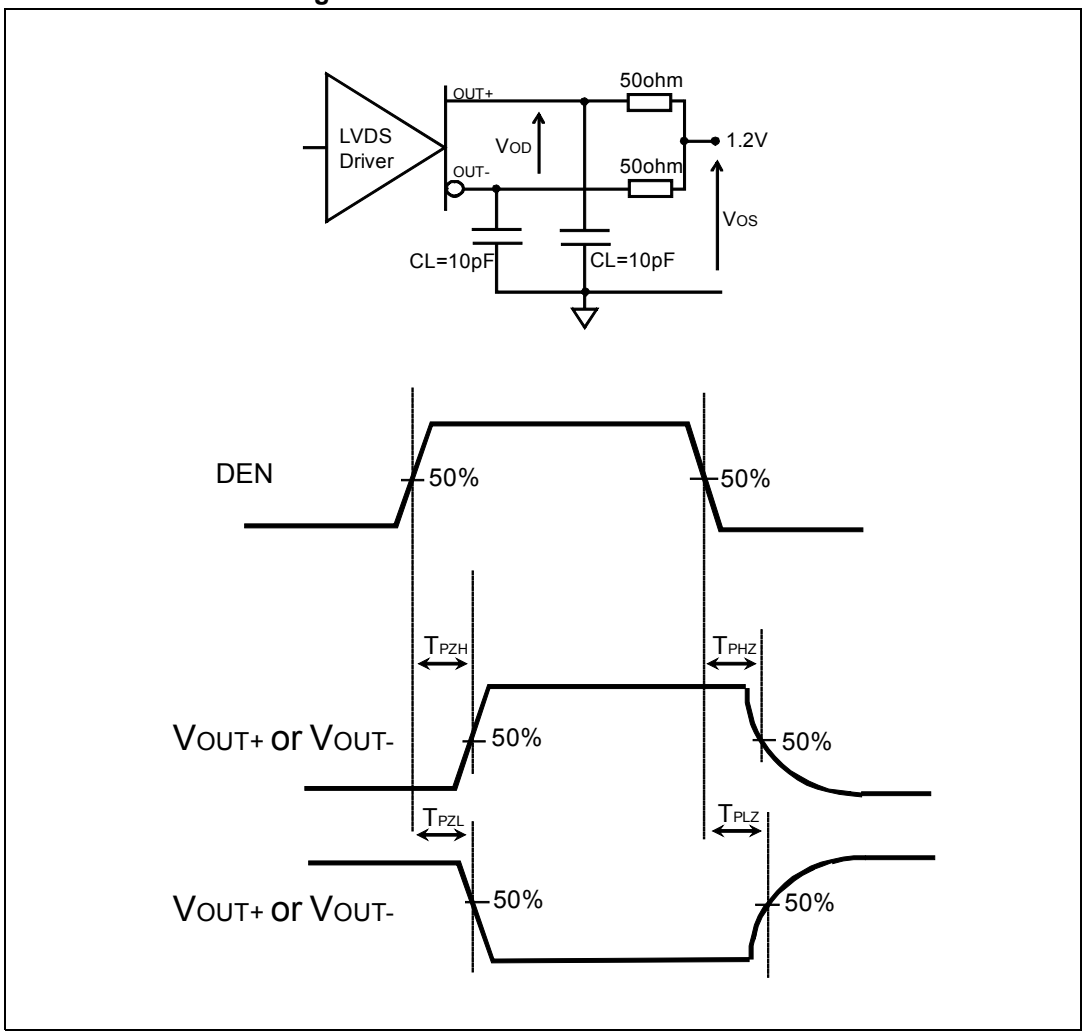


Figure 3. Test circuit, timing and voltage definitions for differential output signal



1. All input pulses are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f = 1 MHz, Z_O = 50 Ω and duty cycle = 50 %.
2. The product is guaranteed in test with CL = 10 pF.

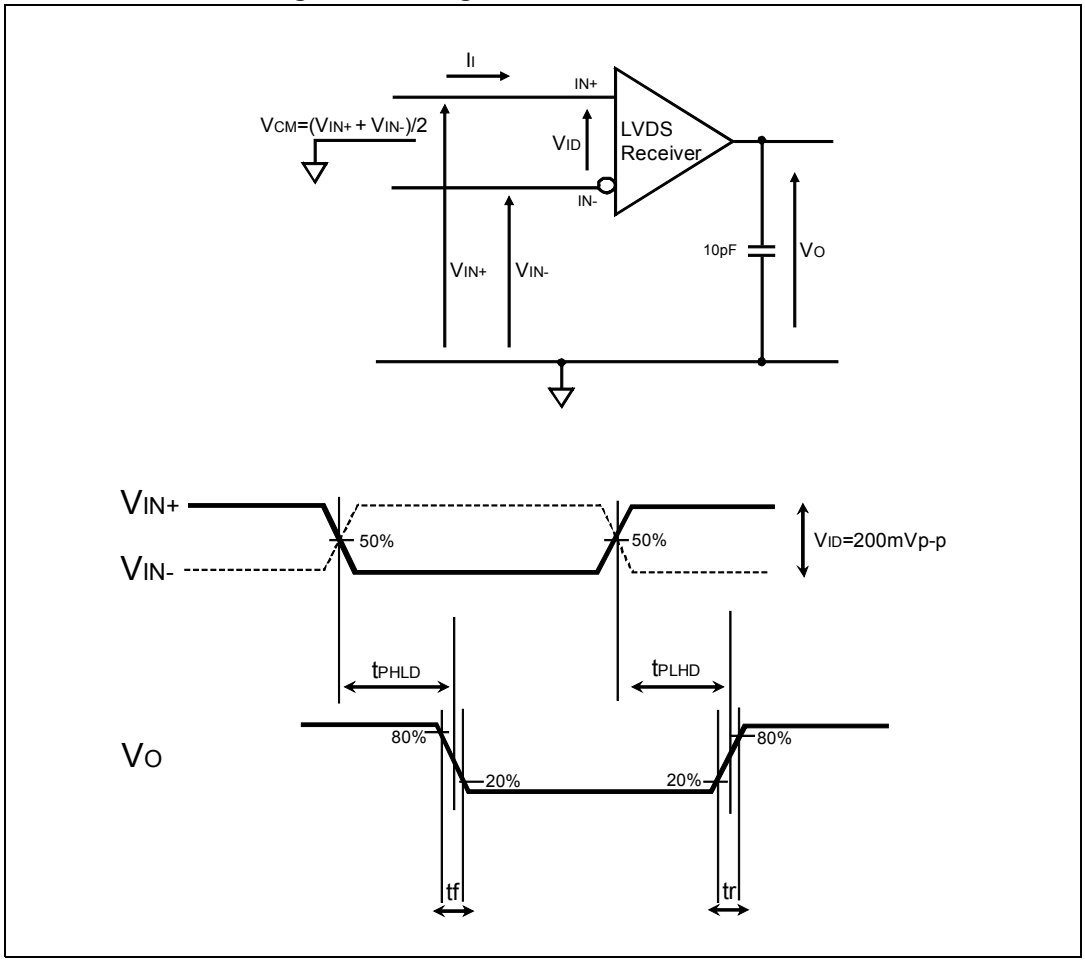
Figure 4. Enable and disable waveforms



1. All input pulses are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f_{REN} or f_{DEN} = 500 kHz, and pulse width REN or DEN = 500 ns.
2. The product is guaranteed in test with CL = 10 pF.

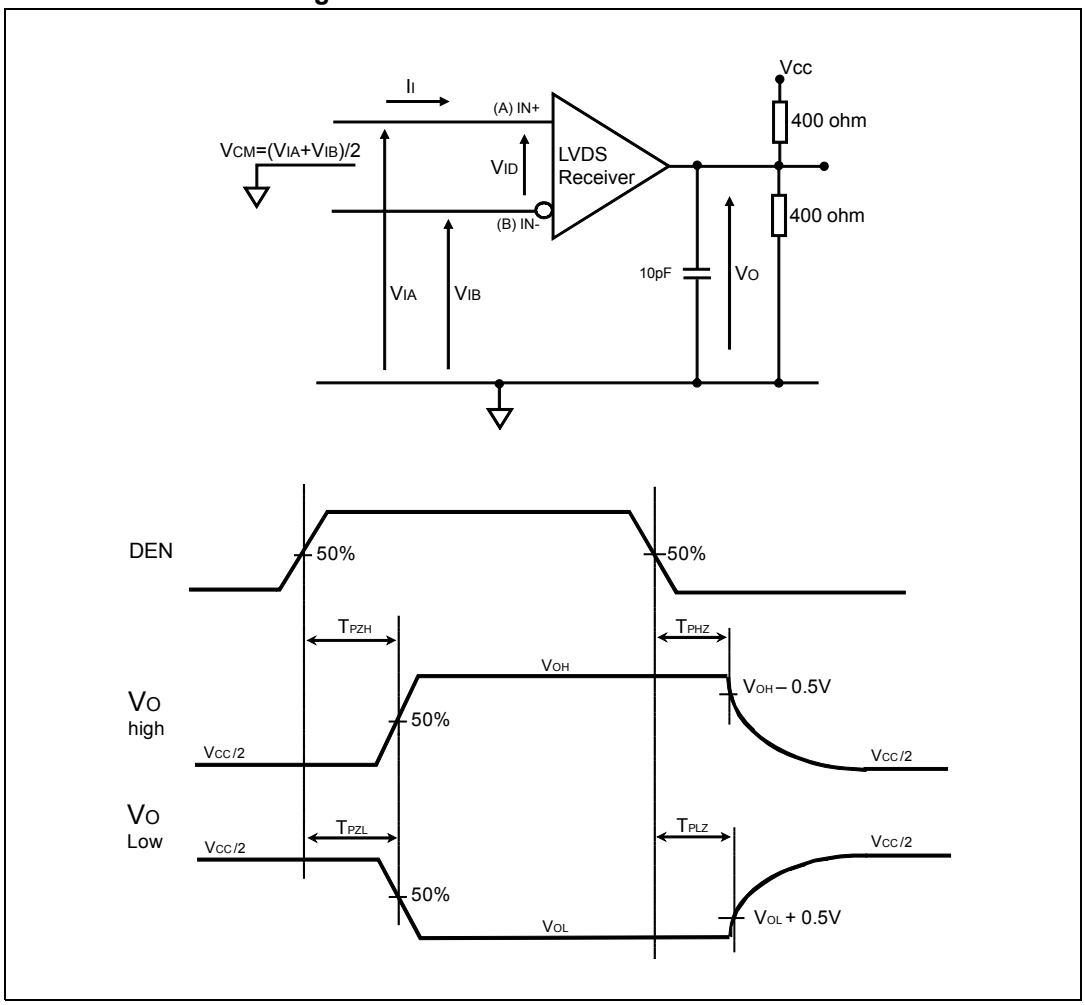
5 Test circuit for the receiver

Figure 5. Timing test circuit and waveforms



1. All input pulses are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f = 1 MHz, Z_O = 50 Ω and duty cycle = 50 %.
2. The product is guaranteed in test with CL = 10 pF.

Figure 6. Enable and disable waveforms



1. All input pulses are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f_G or $f_{\overline{G}}$ = 500 kHz, and pulse width G or $\overline{G}$ = 500 ns.
2. The product is guaranteed in test with CL = 10 pF.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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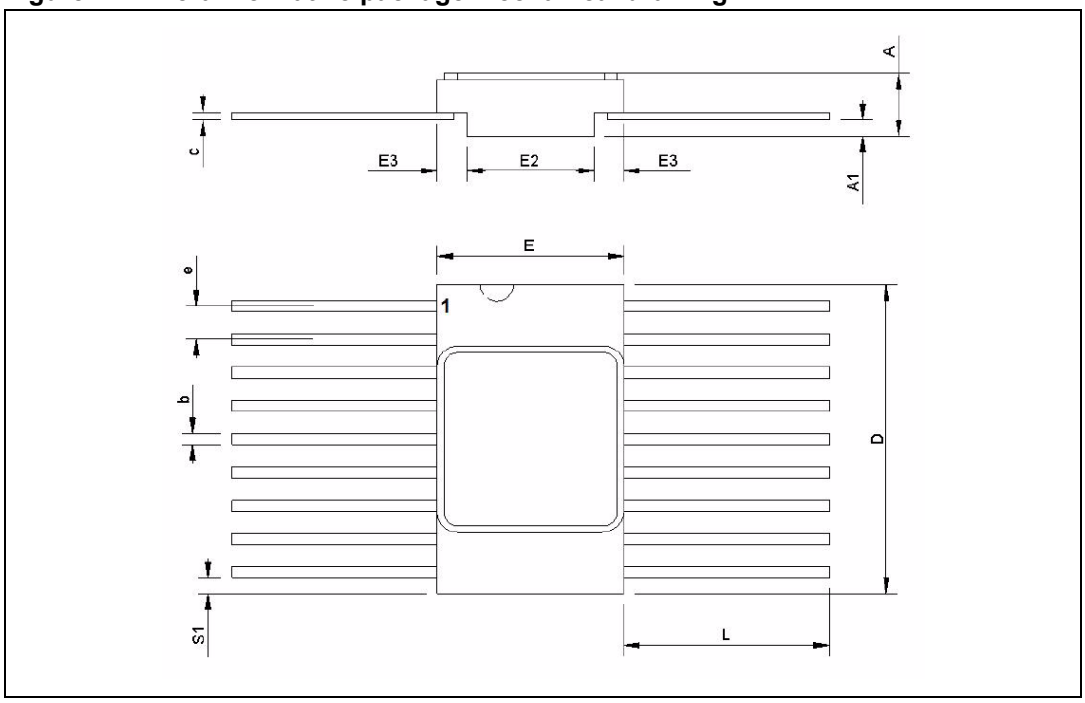
6.1 Ceramic Flat-18 package information

Figure 7. Ceramic Flat 18 package mechanical drawing



1. The upper metallic lid is electrically connected to ground.

Table 8. Ceramic Flat 18 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.46	2.74	0.86	0.097	0.108
A1	0.66	-	-	0.026	-	-
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.14	0.18	0.004	0.005	0.007
D	11.61	11.81	12.01	0.457	0.465	0.473
E	6.99	7.11	7.24	0.275	0.280	0.285
E2	4.67	4.82	4.98	0.184	0.19	0.196
E3	0.76	-	-	0.03	-	-
e	-	1.27	-	-	0.050	-
L	7.37	7.87	8.37	0.290	0.031	0.330
S1	0.13	-	-	0.005	-	-

7 Ordering information

Table 9. Order codes

Order code	Description	Temp. range	Package	Marking(1)	Packing
RHFLVDSR2D2K1	Engineering model	-55 °C to 125 °C	Ceramic Flat-18	RHFLVDSR2D2K1	Strip pack
RHFLVDSR2D2K01V(2)	QML-V flight			TBD	

1. Specific marking only. Complete marking includes the following:
   - SMD pin (on QML-V flight only)
   - ST logo
   - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
   - QML logo (Q or V)
   - Country of origin (FR = France).
2. Not yet in full production

Note: Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

8 Shipping information

Date code

The date code is structured as follows:

- Engineering model: EM xyywwz
- QML flight model: FM yywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Oct-2013	1	Initial release

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