ISL70321SEH, ISL73321SEH

Radiation Hardened Quad Power Supply Sequencers

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The ISL70321SEH and ISL73321SEH are radiation hardened and SEE mitigated power supply sequencers designed to drive Point-of-Load (POL) regulators with enable pins. Up to four power supplies can be fully sequenced by a single device or multiple devices can be easily cascaded to sequence an unlimited number of power supplies for dense RF applications.

This power supply sequencer requires only two feedback resistors per power supply and a single resistor to set the rising and falling delay. The device features precision input comparators with an input threshold voltage of 600mV ±1.5% for the highest possible accuracy when monitoring the power supply voltages.

The ISL70321SEH and ISL73321SEH are offered in an 18 Ld 10mm x 12mm CDFP package or die form and are fully specified across the military ambient temperature range of -55°C to +125°C.

With minimal external component count, precision voltage monitoring, and SET mitigation, the ISL70321SEH and ISL73321SEH are the ideal choice to control many of today's highly dense power systems in high reliability applications.

Applications

- Power sequencing for multi-rail devices such as FPGAs, DSPs, and communications ICs
- Power management of high-density distributed power systems and RF applications

Features

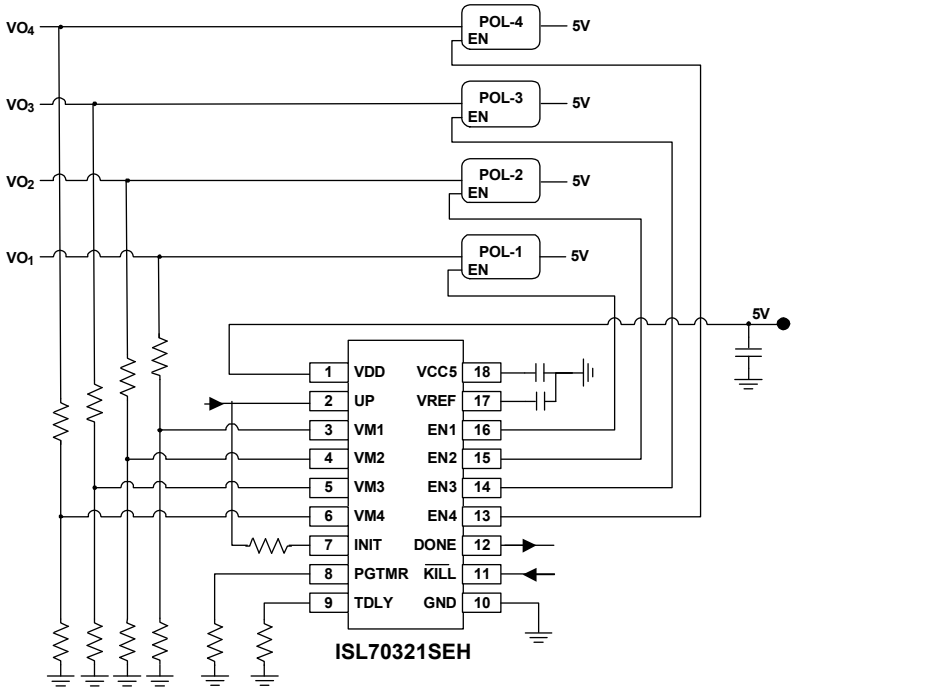
- **Wide operating voltage range, 3V to 13.2V**
- **Single resistor sets the rising and falling delay**
- **Power-off POLs in reverse order or simultaneously**
- **Precision voltage monitoring**
  - **600mV ±1.5% threshold voltage over temperature and radiation**
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Radiation Hardness
  - High Dose Rate (HDR) (50-300rad(Si)/s): 100krad(Si) - ISL70321SEH only
  - Low Lose Rate (LDR) (0.01rad(Si)/s): 75krad(Si) ISL70321SEH and ISL73321SEH
- SEE Hardness (Review SEE Report for details)
  - No SEB/SEL LET_{TH}, V_{DD} = 14.7V: 86MeV•cm^2/mg
  - SET, SEFI free at LET 20MeV•cm^2/mg
- Electrically screened to DLA SMD 5962-17225

Related Literature

- For a full list of related documents, visit our website
  - ISL70321SEH and ISL73321SEH product pages

Table 1. Key Differences Between Family of Parts

Part Number	TID Rating
ISL70321SEH	HDR to 100krad(Si), LDR to 75krad(Si)
ISL73321SEH	LDR to 75krad(Si)



NOTE: DOES NOT INCLUDE PULL-UP RESISTORS ON EN

Figure 1. Typical Application Schematic

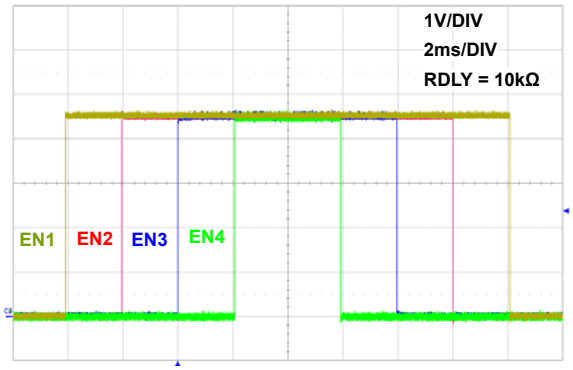


Figure 2. Four Events Up and Down Sequence

Contents

1. Overview

1.1 Functional Block Diagram

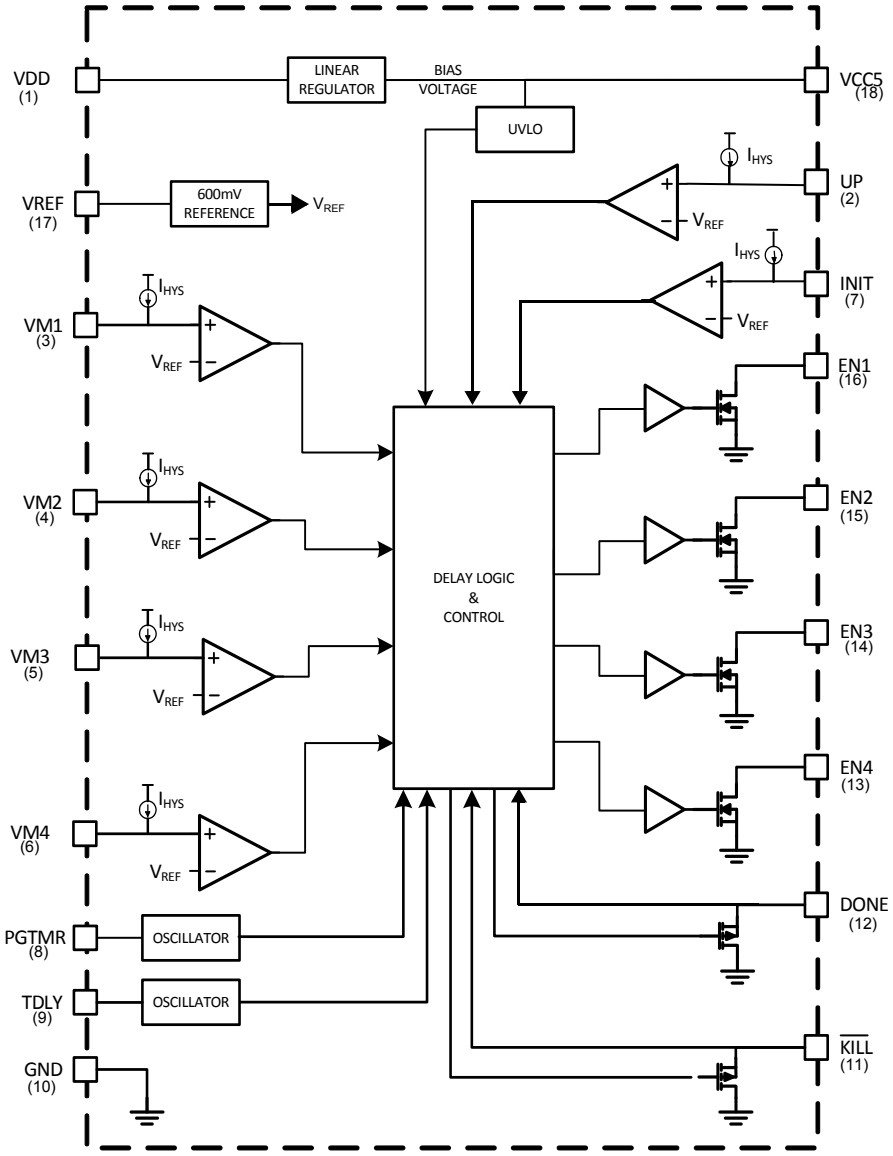


Figure 3. Block Diagram

1.2 Ordering Information

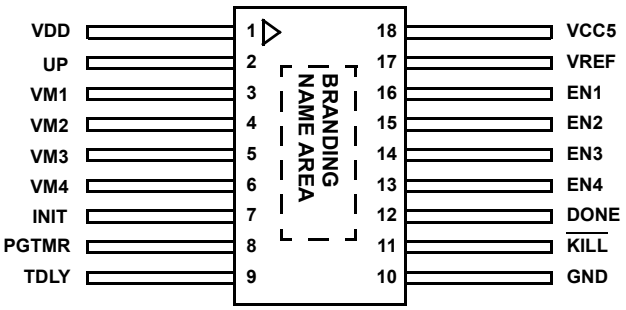
Ordering SMD Number (Note 1)	Part Number (Note 2)	Radiation Hardness (Total Ionizing Dose)	Temperature Range (°C)	Package (RoHS Compliant)	Package Drawing
5962R1722501VXC	ISL70321SEHVF	HDR to 100krad(Si), LDR to 75krad(Si)	-55 to +125	18 Ld CDFP	K18.B
5962R1722501V9A	ISL70321SEHVX		-55 to +125	Die	N/A
N/A	ISL70321SEHF/PROTO (Note 3)	N/A	-55 to +125	18 Ld CDFP	K18.B
N/A	ISL70321SEHX/SAMPLE (Note 3)	N/A	-55 to +125	Die	N/A
5962L1722502VXC	ISL73321SEHVF	LDR to 75krad(Si)	-55 to +125	18 Ld CDFP	K18.B
5962L1722502V9A	ISL73321SEHVX		-55 to +125	Die	N/A
N/A	ISL70321SEHEV1Z (Note 4)	Single IC Evaluation Board			
N/A	ISL70321SEHEV2Z (Note 4)	Dual IC Evaluation Board			
N/A	ISL70321SEHDEMO1Z (Note 4)	Single IC Demonstration Board			

Notes:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.
4. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

1.3 Pin Configuration

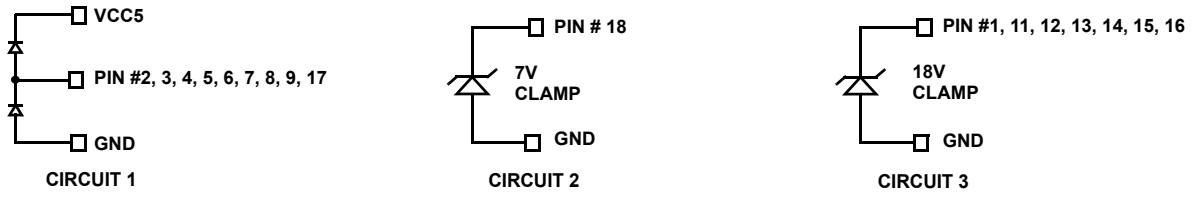
ISL70321SEH / ISL73321SEH
(18 Ld CDFP)
Top View



NOTE: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.4 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VDD	3	Supply for internal linear regulator of the ISL70321SEH. The supply to VDD should be locally bypassed using at least a 0.1µF ceramic capacitor.
2	UP	1	Commands the ISL70321SEH to sequence the power supplies up or down. This pin has an identical type structure as the VM_X pins. This pin can be driven by a system controller or used to sense a non-sequenced power supply voltage to start the power-up sequence.
3, 4, 5, 6	VM1 - VM4	1	Voltage monitor inputs. This is a comparator type input with a rising threshold of 600mV and programmable hysteresis through current I_{HYS}. Connect this pin to an external resistor divider between each sequenced power supply and GND. During power-up sequencing, driving this pin above 600mV indicates that the sequenced power supply has reached the desired power-on voltage. During power-down sequencing, a voltage below 600mV indicates that the sequenced power supply has reached the desired power-off voltage.
7	INIT	1	Sequence INITIATE pin. When using the device in a stand-alone or the first in a cascade configuration, connect this pin to UP. When not the first IC in a cascade configuration, this input is driven by the DONE output pin of the previous ISL70321SEH. This pin has an identical type structure as the VM_X pins. See "Applications Information" on page 16 for more information on this pin's configuration in cascaded applications.
8	PGTMR	1	A resistor connected between PGTMR to GND sets the time allowed for a power supply to reach a power-good state after being enabled with ENx. Power-good timer is adjusted from 4ms to 40ms by a 10kΩ to 100kΩ resistor. Connect this pin to VCC5 to disable the power-good timer.
9	TDLY	1	A resistor connected between TDLY and GND sets the rising and falling time delay between a supply ON/OFF signal (UP or VMx) and the enabling or disabling of (ENx) of the next power supply in the sequence. Delay timer can be adjusted from 2ms to 20ms by a 10kΩ to 100kΩ resistor. Connect this pin to VCC5 if no assured delay is required between supplies being sequenced on or off.
10	GND	1, 2, 3	Connect this pin to the PCB ground plane.
11	$\overline{KILL}$	3	This pin is both an input and an output. Disable all outputs simultaneously by pulling $\overline{KILL}$ low. Open-drain output indicating a fault condition. After a fault clear, $\overline{KILL}$ must be high before subsequent UP driven high.
12	DONE	3	Open-drain indicator that device has successfully sequenced on (DONE is high) or off (DONE is low) all the power supplies. DONE is low when sequence up has not completed.
13, 14, 15, 16	EN4 - EN1	3	These pins are open-drain outputs. Use an external pull-up resistor and connect to the enable pin of each power supply being sequenced.
17	VREF	1	Output of the internal 600mV reference voltage. Bypass this pin to the PCB ground plane with a 220nF ceramic capacitor located as close as possible to the pin.
18	VCC5	2	Output of the internal linear regulator and provides bias to all internal circuitry. Locally filter this pin to GND using a 470nF ceramic capacitor as close as possible to the pin.



1.5 Typical Application Schematic

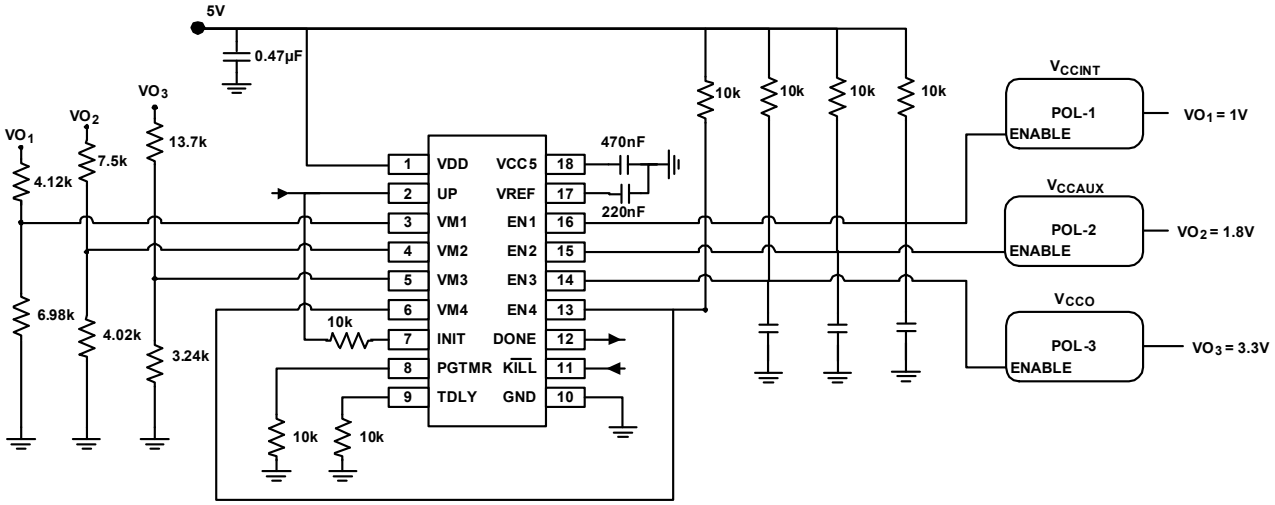


Figure 4. Radiation Hardened FPGA Power Sequencer Solution

1.6 Timing Diagrams

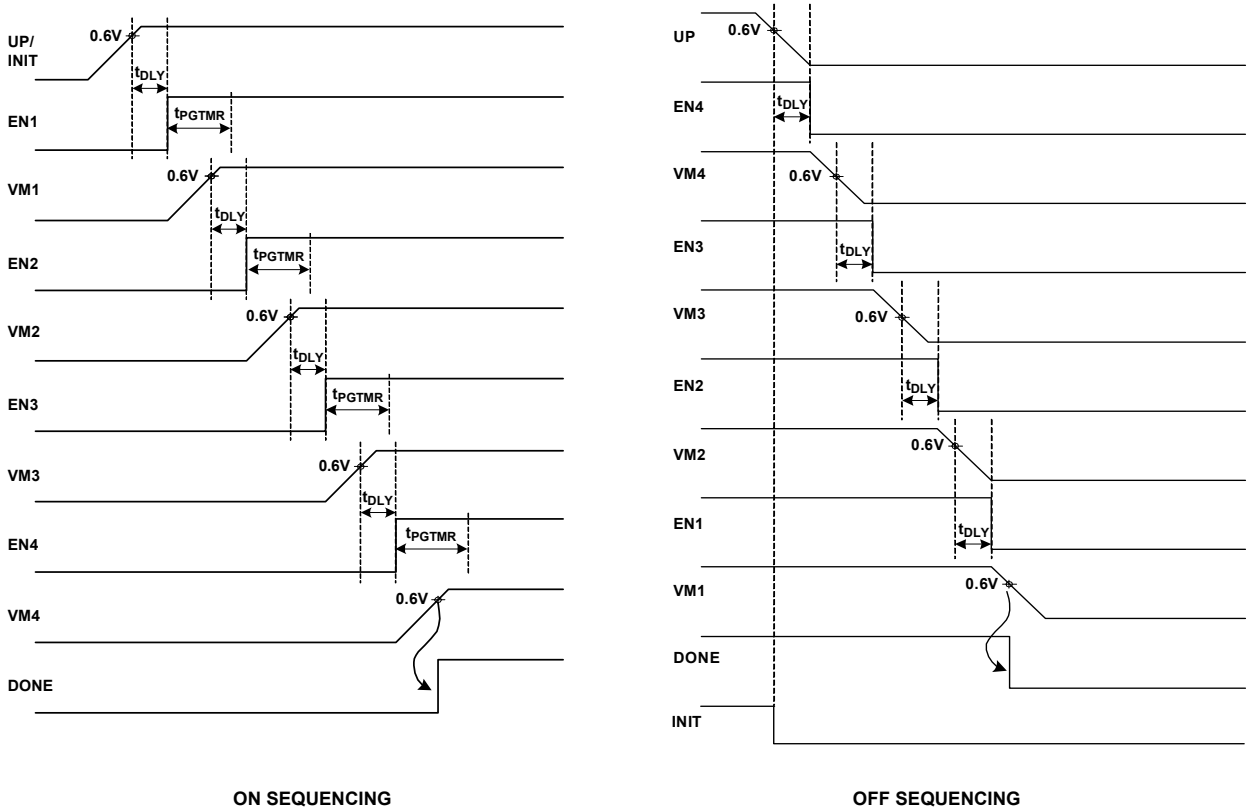


Figure 5. Sequence Up and Sequence Down Timing Diagrams

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VDD	GND - 0.3	GND + 16	V
ENX, $\overline{KILL}$, DONE (VDD < 5V)	GND - 0.3	GND + 12	V
ENX, $\overline{KILL}$, DONE (VDD ≥ 5V)	GND - 0.3	GND + 16	V
VDD in Ion Beam	GND - 0.3	GND + 14.7	V
VCC5		6.5	V
		200 (I_{OUT})	mA
VREF	Do Not Load, loading lowers the VREF		
UP, VM_X, PGTMR, TDLY, INIT	GND - 0.3	VCC5 + 0.3	V
ENX, $\overline{KILL}$, DONE, INIT		-15 (Pull Down Current)	mA
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015.7)	8		kV
Machine Model (Tested per JESD22-A115C)	300		V
Charged Device Model (Tested per JS-002-2014)	1		kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CDFP Package K18.B (Notes 5, 6)	73	3

Notes:
5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
6. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-55	+125	°C
VDD	3.3 ±10%	12 ±10%	V
Timer Delay Resistors	10	100	kΩ
VDD Capacitor	≥100	-	nF
VREF Capacitor	220 ±20%	220 ±20%	nF
VCC5 Capacitor	470 ±20%	470 ±20%	nF

2.4 Electrical Specifications

Unless otherwise noted, V_{DD} = 3V - 13.2V; ENx, DONE, $\overline{KILL}$ are pulled up to VDD with a 10kΩ resistor; PGTMR, TDLY are connected to ground with a 10k resistor; VREF is bypassed to GND with a 220nF capacitor, VCC5 is bypassed to GND with a 470nF capacitor; $T_A = T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70321SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
VDD Power Supply						
3V Quiescent Supply Current	IDDQ_3	UP and INIT = 0.5V		3.5	**6**	mA
13.2V Quiescent Supply Current	IDDQ_13	UP and INIT = 0.5V		4.8	**8**	mA
3V Operating Supply Current	IDD_3	UP and INIT = 0.7V with EN tied to VM to 5V		3.5	**6**	mA
13.2V Operating Supply Current	IDD_13	UP and INIT = 0.7V with EN tied to VM to 5V		4.9	**8**	mA
Rising Undervoltage Lockout	UVLO	V_{DD} rising to V_{REF} rising, VCC5 = 45mA	**2.8**	2.88	**2.95**	V
Undervoltage Lockout Hysteresis	UVLO hys	UVLO - V_{DD} falling to V_{REF} turn-off	**30**	71	**100**	mV
Time from VDD to Inputs being Active	t_{VDD_INPUT}	V_{DD} rising to inputs active, t_{DLY} timer disabled		2.1	**3**	ms
VCC5 Linear Regulator						
Output Voltage	VCC5	V_{DD} = 13.2V, I_{LOAD} = 45mA	**4.5**	5.0	**5.5**	V
Current Limit on VCC5	I_{LIM}		**50**		**200**	mA
Reference Voltage						
Reference Voltage	V_{REF}		**594**	600	**606**	mV
INIT, UP, VMx (VM1 -VM4) Comparator Inputs						
Comparator Rising Threshold Voltage	V_{TH}		**591**	601	**609**	mV
Comparator Input Leakage Current	I_{LK}	$V_{UP} = V_{VMx}$ = 0.5V	**-50**	5	**50**	nA
Hysteresis Current	I_{HYS}	$V_{UP} = V_{VMx}$ = 0.7V	**-28**	-24	**-20**	µA
Timer Disabled Delay Time from VM, UP, INIT Inputs to EN Output	$DIST_{VM\_EN\ dly}$	t_{DLY} = VCC5 rising VM > VM V_{TH} to EN rising start	**1.5**	3.8	**4.5**	µs
Enable (EN1 - EN4) Outputs						
ENx Drive (Sink) Current	I_{ENS}	V_{DD} = 3V, V_{ENx} = 0.4V	**8**			mA
ENx Leakage Current	I_{ENLK}	$V_{DD} = V_{ENx}$ = 13.2V		0.01	**0.3**	µA
DONE Input/Output						
Drive (Sink) Current	I_{DNS}	V_{DD} = 3V, V_{DONE} = 0.4V	**8**			mA
Leakage Current	I_{DNLK}	$V_{DD} = V_{DONE}$ = 13.2V		3.3	**5**	µA
Input Vth for ‘LOW’	V_{IL}		**0.8**	0.98		V
Input Vth for ‘HIGH’	V_{IH}			1.04	**1.4**	V
Delay and Power-Good Timer						
10kΩ Delay Timer	t_{DLY_10}	t_{DLY} resistor = 10kΩ	**1.8**	2	**2.2**	ms
100kΩ Delay Timer	t_{DLY_100}	t_{DLY} resistor = 100kΩ	**18**	20	**22**	ms
10kΩ Power Good Timer	t_{PG_10}	PGTMR resistor = 10kΩ	**3.6**	4	**4.4**	ms
100kΩ Power Good Timer	t_{PG_100}	PGTMR resistor = 100kΩ	**36**	40	**44**	ms

Unless otherwise noted, V_{DD} = 3V - 13.2V; ENx, DONE, $\overline{KILL}$ are pulled up to VDD with a 10kΩ resistor; PGTMR, TDLY are connected to ground with a 10k resistor; VREF is bypassed to GND with a 220nF capacitor, VCC5 is bypassed to GND with a 470nF capacitor; $T_A = T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70321SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
$\overline{KILL}$ Input/Output						
Drive (Sink) Current	I_{KS}	V_{DD} = 3V, $V_{\overline{KILL}}$ = 0.4V	**7**			mA
Leakage Current	I_{KLK}	V_{DD} = $V_{\overline{KILL}}$ = 13.2V		3.2	**5**	µA
Input Vth for ‘LOW’	V_{IL}	V_{DD} = 3V	**0.8**	0.98		V
Input Vth for ‘HIGH’	V_{IH}	V_{DD} = 3V		0.99	**1.4**	V
Minimum Time to Trigger a $\overline{KILL}$ Input	t_{KON}			0.5	**1.4**	µs
Delay from $\overline{KILL}$ low to EN1 - EN4 Low	t_{KDLY}			1	**1.6**	µs
VM < 0.591V to $\overline{KILL}$ Low	t_{KRESP}			0.9	**1.6**	µs

Notes:

7. Typical values shown are not guaranteed.
8. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.

3. Typical Performance Curves

Unless otherwise noted, V_{DD} = 12V; ENx, DONE, $\overline{KILL}$ are pulled up to VCC5 with a 10k resistor; TDLY and PGTMR resistors are 10k; VREF and VCC5 are bypassed to GND with a 220nF, and a 470nF capacitor, respectively; T_A = +25°C

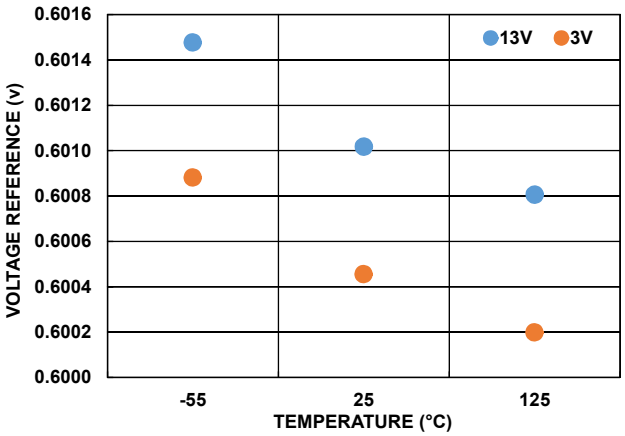


Figure 6. V_{REF} Over Temperature and Bias Voltage

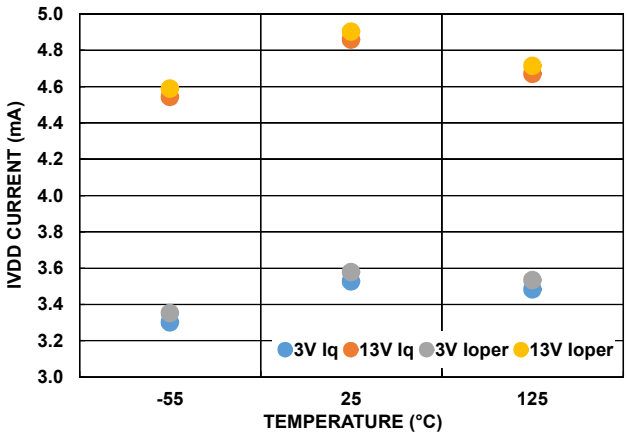


Figure 7. V_{DD} Current Over Temperature and Bias Voltage

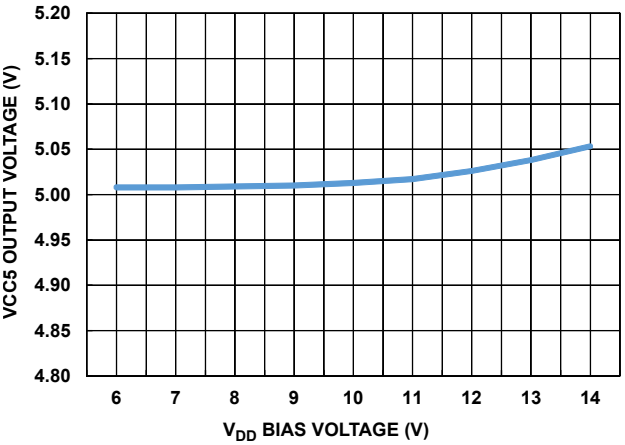


Figure 8. VCC5 at 45mA Current Output vs Bias Voltage

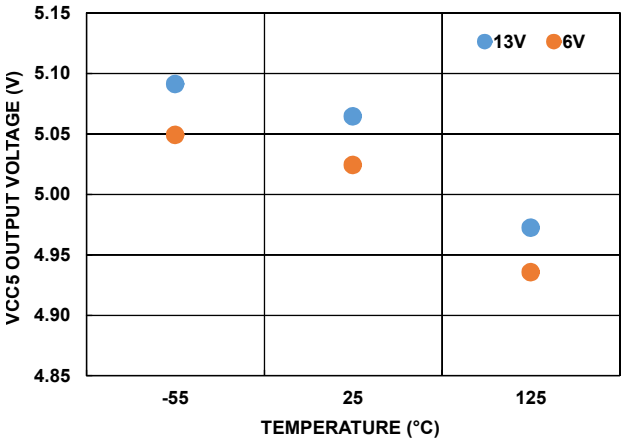


Figure 9. VCC5 at 45mA Current Output vs Bias Voltage

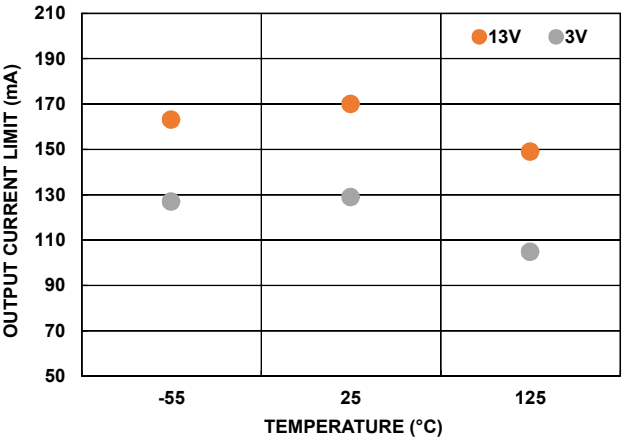


Figure 10. VCC5 Current Limit Over Temperature

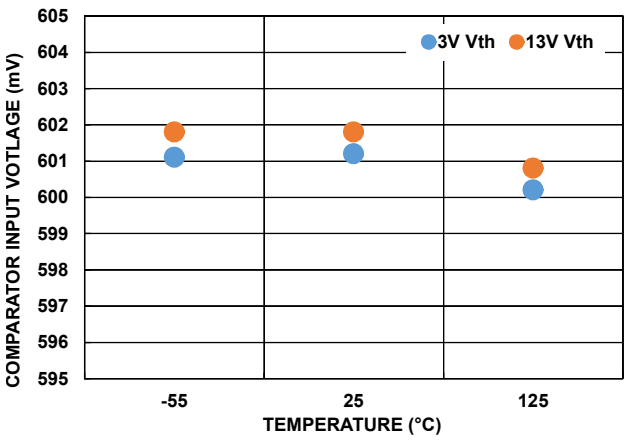


Figure 11. VMx, INIT, UP Comparator Rising Vth

Unless otherwise noted, V_{DD} = 12V; ENx, DONE, $\overline{KILL}$ are pulled up to VCC5 with a 10k resistor; TDLY and PGTMR resistors are 10k; VREF and VCC5 are bypassed to GND with a 220nF, and a 470nF capacitor, respectively; T_A = +25°C **(Continued)**

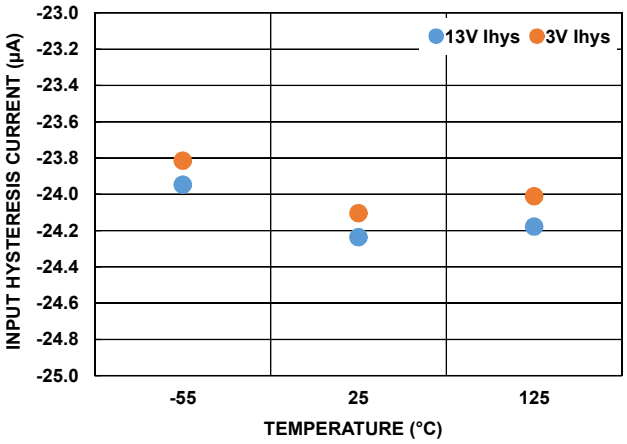


Figure 12. VMx, INIT, UP Hysteresis Current

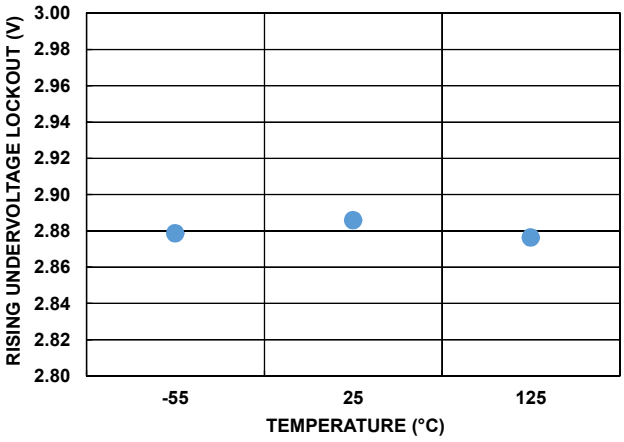


Figure 13. UVLO vs Temperature

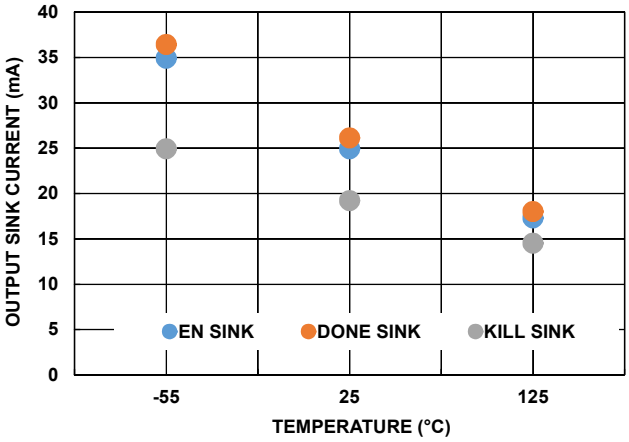


Figure 14. EN, DONE, $\overline{KILL}$ Sink Current

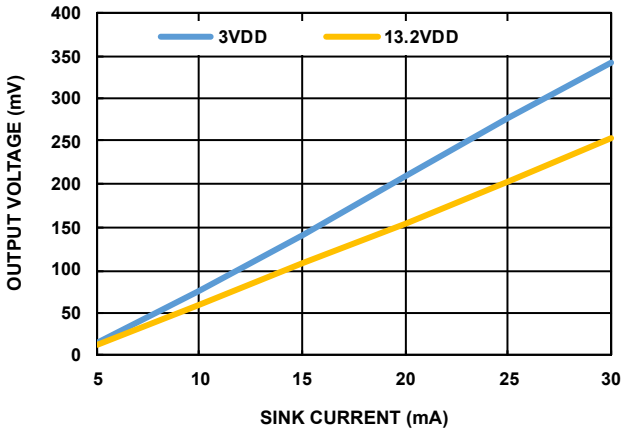


Figure 15. DONE, ENx, $\overline{KILL}$ VOL vs ISINK

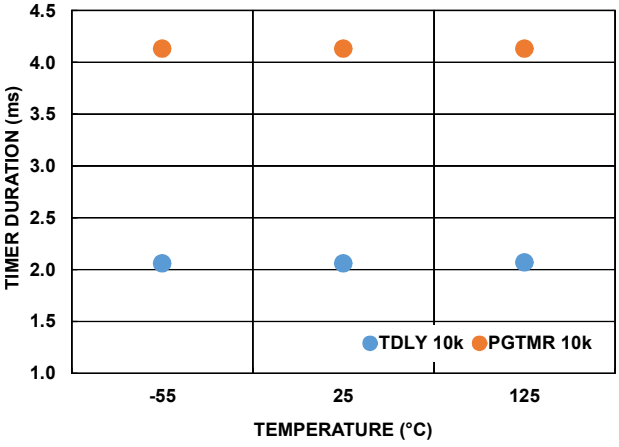


Figure 16. DELAY and PGOOD Timer Over Temperature (10kΩ)

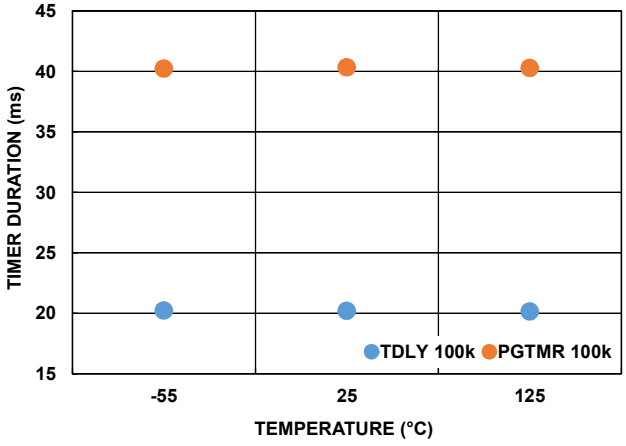


Figure 17. DELAY and PGOOD Timer Over Temperature (100kΩ)

Unless otherwise noted, V_{DD} = 12V; ENx, DONE, $\overline{KILL}$ are pulled up to VCC5 with a 10k resistor; TDLY and PGTMR resistors are 10k; VREF and VCC5 are bypassed to GND with a 220nF, and a 470nF capacitor, respectively; T_A = +25°C **(Continued)**

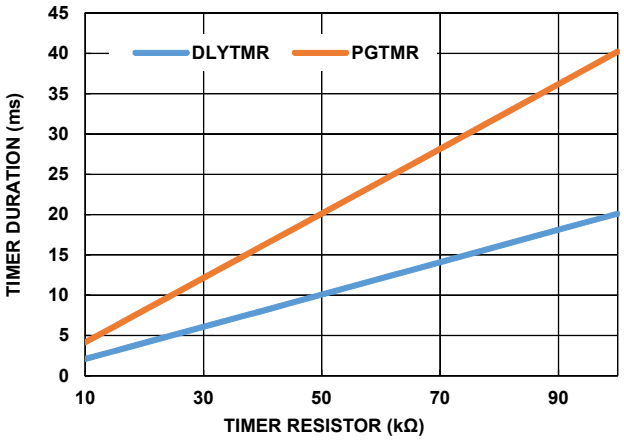


Figure 18. DELAY and PGOOD Timer Linearity

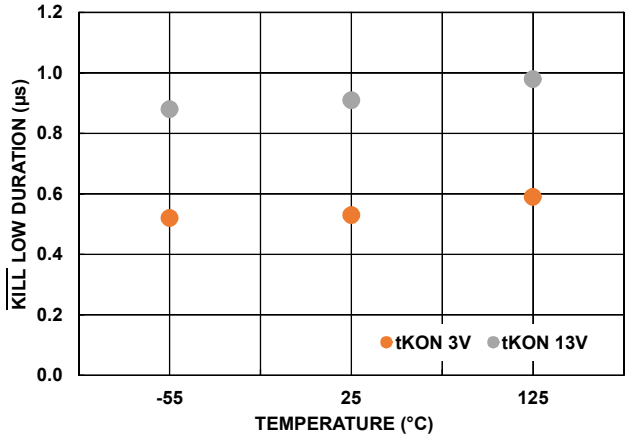


Figure 19. Minimum $\overline{KILL}$ Time

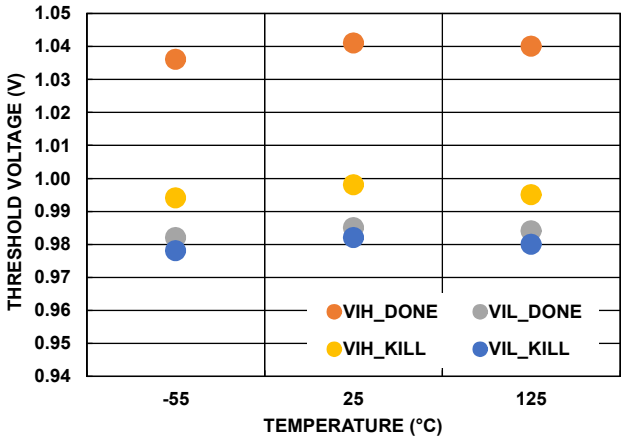


Figure 20. DONE, $\overline{KILL}$ Threshold Voltage

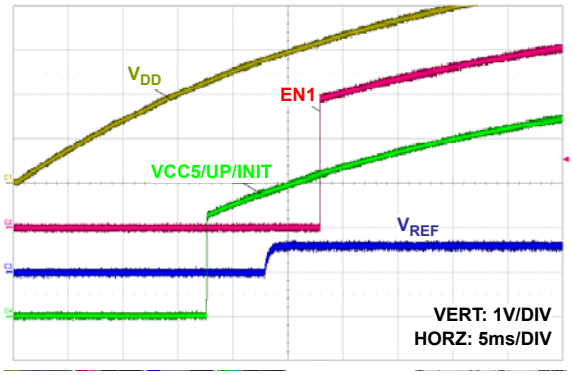


Figure 21. V_{DD} Rising to VCC5, V_{REF} and EN1 Transition

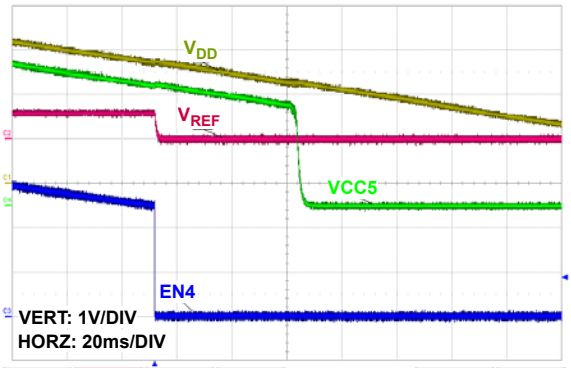


Figure 22. V_{DD} Falling to VREF EN4 VCC5 Transitions

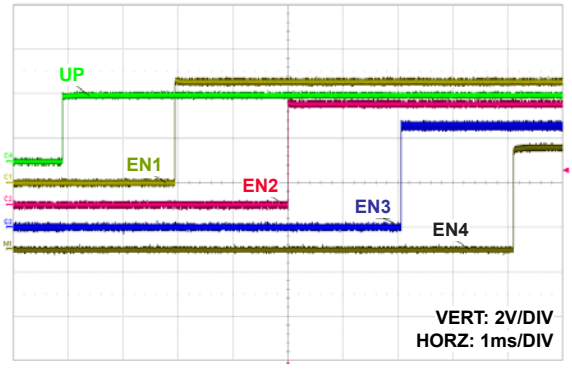


Figure 23. UP to EN1 Through EN4 Transitions, 10k t_{DLY} Resistor (2ms)

Unless otherwise noted, V_{DD} = 12V; ENx, DONE, $\overline{KILL}$ are pulled up to VCC5 with a 10k resistor; TDLY and PGTMR resistors are 10k; VREF and VCC5 are bypassed to GND with a 220nF, and a 470nF capacitor, respectively; T_A = +25°C **(Continued)**

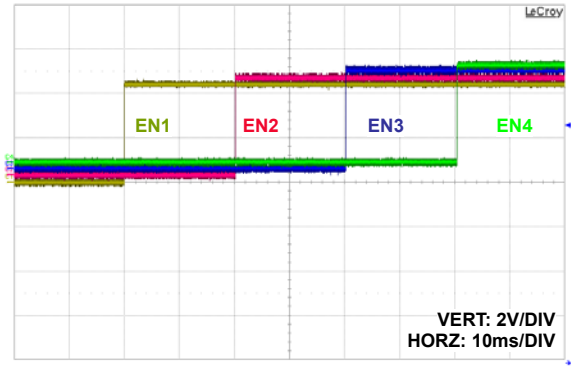


Figure 24. EN1 Through EN4 Transitions with 100k t_{DLY} (20ms)

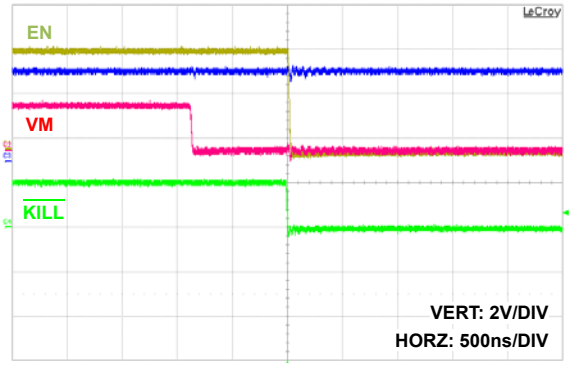


Figure 25. VM Input Fault to $\overline{KILL}$

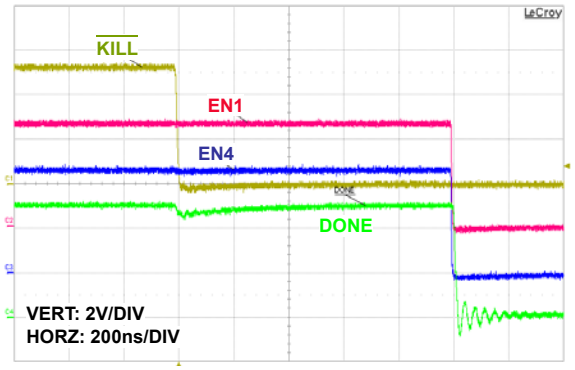


Figure 26. $\overline{KILL}$ Input to Outputs

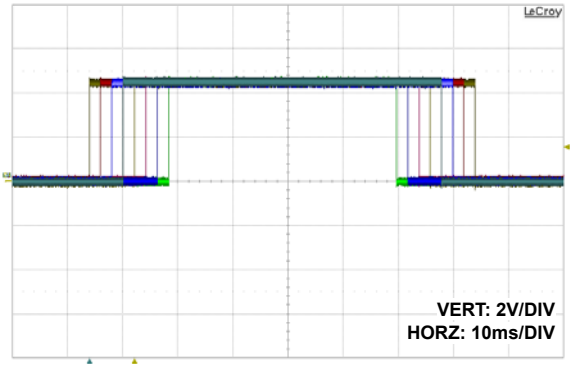


Figure 27. Dual ISL70321SEH 8-Event Sequence Up/Down

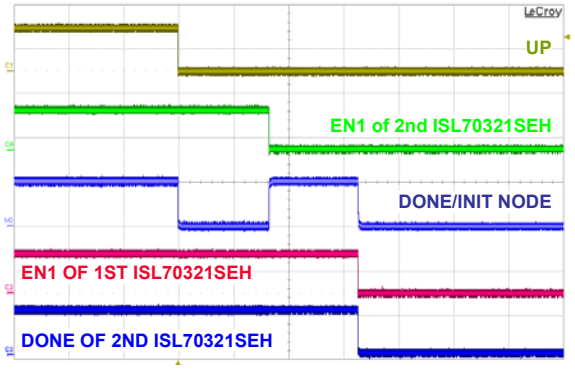


Figure 28. Dual ISL70321SEH Down Sequence Handshake Signals

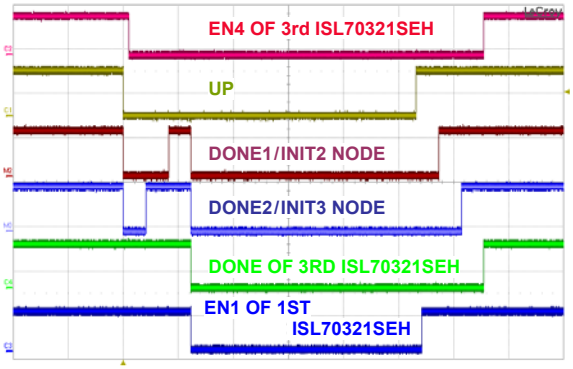


Figure 29. Triple ISL70321SEH Handshake Signals

4. Functional Description

The ISL70321SEH and ISL73321SEH are radiation hardened and SEE mitigated sequencer circuits designed to drive multiple Point-of-Load (POL) regulators with active high enable inputs. Up to four individual sequenced events can be controlled by a single device or by cascading multiple devices increase to an unlimited number of sequenced events.

This power supply sequencer requires only two feedback resistors for output voltage sensing per sequenced power supply; a single resistor to set the rising and falling delay between sequenced supplies, and an additional single resistor for setting the power-good timer of each sequenced supply. This device features input comparators with an input offset voltage ≤3mV and ±1% threshold voltage reference to achieve precision voltage monitoring.

After an adequate V_{DD} bias voltage is applied, and with both the UP and INIT inputs high, the ISL70321SEH and ISL73321SEH will initiate the first event in the sequence by releasing EN1 to be pulled high through an external pull-up resistance. The output of the connected POL is then monitored for an adjustable threshold level by VM1 and when deemed ‘good’ within the power-good timer period, EN2 is released to be pulled high. This process is repeated until EN4 is released and the DONE output is finally released, signifying the sequence up is complete. The DONE output remains high and is pulled to GND after sequence down is completed.

The UP pin commands the IC to sequence up or down the power supplies using the ENx outputs. The UP detection circuitry is identical to the VMx pins and can be driven by a system controller to determine whether the sequence is up or down.

The INIT pin is the initiator of either an up or down sequence event chain. The INIT detection circuitry is identical to the VMx pins and can be driven by a system controller to initiate the up or down sequence activity.

To sequence down, the UP and INIT are pulled low and during sequence down, the device deasserts the EN4 to EN1 outputs in that order (reverse from sequence up) after the voltages on pin VM4 to VM1 fall below their programmed thresholds.

This describes the basic operation of a single ISL70321SEH or ISL73321SEH IC, a multiple IC configuration will be described later in this document.

The rising and falling delay, t_{DLY}, can be programmed in the range of 2ms to 20ms using a single resistor (10kΩ to 100kΩ) from TDLY to GND. The rising delay is from VM_X crossing its threshold to EN_{X+1} being released. There is also a delay from UP crossing its threshold and EN1 being released. During power-down, falling delay is from VM_N falling below the threshold to EN_{N-1} being asserted low. There is also a delay from UP falling below the threshold and EN4 asserted low.

A PGOOD timer, t_{PGTMR}, in the range of 4ms to 40ms can be programmed using a resistor (10kΩ to 100kΩ) from PGTMR to GND. This is the amount of time from turn-on that a power rail has to cross the threshold. The PGOOD timer is active only during power-up sequencing and starts counting after each ENx pin is released to go high.

A comprehensive fault suite has been designed into ISL70321SEH and ISL73321SEH and is described in “Fault Monitoring” on page 18.

5. Applications Information

5.1 Undervoltage Lockout

The VDD pin accepts the required supply voltage range of 3V to 13.2V and is the input to the internal linear regulator. VCC5 is the output of the regulator and is equal to 5V when V_{DD} > 5V and tracks V_{DD} when 3V < V_{DD} < 5V. VCC5 provides the bias for all internal circuitry of the sequencer. An UVLO circuitry monitors the voltage on VCC5. When the voltage is above ~2.8V, the ISL70321SEH and ISL73321SEH initialize by turning on the 600mV band gap reference voltage and the internal power-good and delay timer oscillators. If the voltage on VCC5 falls below 2.8V, the device shuts off both oscillators and the band-gap reference. It also holds the open-drain ENx outputs low until VCC5 drops below 1.2V.

5.2 Selecting the VM_X Feedback Resistors

As shown in Figure 30, the voltage monitoring circuit features a comparator type input. This circuit allows the level of the sequenced power supply output voltage to precisely gate the turn-on/turn-off of the next regulator. The internal I_{HYS} current source with a typical value of 24µA, is only active when the voltage on the VM_X pin is above the V_{REF} threshold and serves to add hysteresis between the turn-on and turn-off levels. As the sequenced power supply voltage rises, the turn-on level (V_{ON}), is set by the resistor divider (R_1 and R_2) from V_{OUTx}. During power-down, the turn-off (V_{OFF}) level is set by the resistor divider and the internal source current, I_{HYS}.

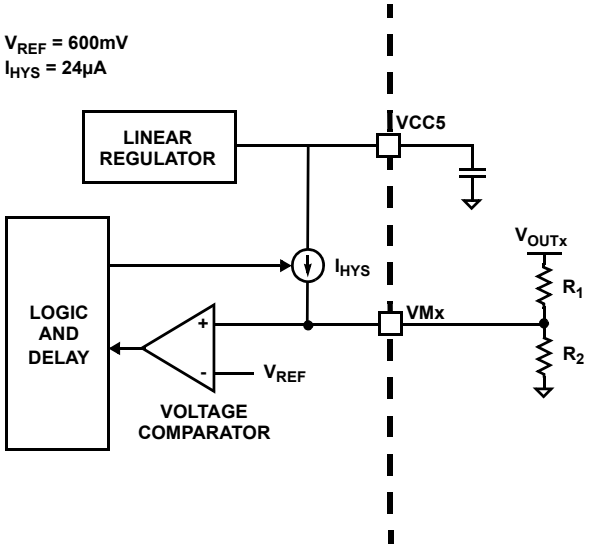


Figure 30. Voltage Monitor Circuit

(EQ. 1) defines the relationship between the resistor divider and VM_X turn-on level (V_{ON}).

$$V_{ON} = V_{REF} \cdot \left[1 + \frac{R_1}{R_2}\right] \quad \text{(EQ. 1)}$$

Once the voltage at the VM_X pin reaches the turn-on threshold, the I_{HYS} current source turns on.

The turn-off level (V_{OFF}) is set by the resistor divider network and I_{HYS} and is defined by (EQ. 2).

$$V_{OFF} = V_{ON} - (I_{HYS} \cdot R_1) \quad \text{(EQ. 2)}$$

The resistor induced difference between the turn-on and turn-off levels provides adjustable hysteresis.

To calculate the resistors, first determine the V_{ON} and V_{OFF} levels. Then use (EQ. 3) to calculate R_1:

$$R_1 = \frac{V_{ON} - V_{OFF}}{I_{HYS}} \quad \text{(EQ. 3)}$$

With R_1 determined, use (EQ. 4) to calculate R_2:

$$R_2 = \frac{R_1 \cdot V_{REF}}{V_{ON} - V_{REF}} \quad \text{(EQ. 4)}$$

5.2.1 Resistor Calculation Example

Using Figure 4 on page 7 as a reference in this example, the monitored POL-2 voltage is 1.8V. During sequencing up, POL-3 should turn on when POL-2 reaches 95% of its nominal voltage and during sequencing down, POL-1 should turn off when POL-2 falls below 85% of its nominal voltage.

The accuracy of the monitored voltages will be affected by the tolerances of the resistor. It is recommended to use 1% tolerance resistors to optimize performance.

With V_{ON} and V_{OFF} are determined to be 1.71V and 1.53V, respectively, use (EQ. 3) to calculate R_1.

$$R_1 = \frac{1.71V - 1.53V}{24\mu A} = 7.5k\Omega$$

Now that R_1 is calculated, use (EQ. 4) to calculate R_2:

$$R_2 = \frac{7.5k\Omega \cdot 600mV}{1.71V - 600mV} = 4.05k\Omega$$

With the resistor divider calculated the next step would require choosing the closest standard resistor values and double checking V_{ON} and V_{OFF} with (EQ. 1) and (EQ. 2). Using a 7.5kΩ for R_1 and 4.02kΩ for R_2 results in:

$$V_{ON} = 600mV \cdot \left[1 + \left(\frac{7.5k\Omega}{(4.02k\Omega)}\right)\right] = 1.71V$$

$$V_{OFF} = 1.71V - (24\mu A \cdot 7.5k\Omega) = 1.53V$$

5.3 Selecting the Sequence Delay Resistor

During the up sequence, the resistor (10kΩ to 100kΩ) R_{DLY} is used to divide down the internal oscillator, which sets the delay between the time a power supply crosses its programmed turn-on threshold and the subsequent power supply being enabled. During sequence down, the oscillator adds a delay from the time a power supply reaches the programmed turn-off threshold and the disabling of the next power supply.

The delay range is from 2ms to 20ms and RDLY can be calculated with (EQ. 5):

$$R_{DLY}(k\Omega) = \text{DELAY TIME (ms)} \cdot 5000 \quad \text{(EQ. 5)}$$

If no delay is required during power-up and down, TDLY can be connected to VCC5. The accuracy of the delay will be affected by the tolerance of the resistor. It is recommended to use 1% tolerance resistors.

5.4 Selecting the PGOOD Timing Resistor

During the power-up sequence, resistor R_{TMR} can be used to program the time a power supply is required to reach the desired turn-on level once it has been enabled. This PGOOD timer is reset each time a power supply crosses the threshold on VM1 - VM4.

The PGOOD timer range is 4ms to 40ms and R_{TMR} can be calculated with (EQ. 6):

$$R_{PGTMR}(k\Omega) = \text{DELAY TIME (ms)} \cdot 2500 \quad \text{(EQ. 6)}$$

The PGOOD timer is not active during power-down sequencing. If no PGOOD counter is required during power-up, PGTMR can be shorted to VCC5. The accuracy of the counter will be affected by the tolerance of the resistor. It is recommended to use 1% tolerance resistors.

Table 2. Resistor vs Delay and Power Good Timer Duration

Resistor (kΩ)	t_{DLY} (ms)	PGTMR (t_{DLY}) (ms)
10	2	4
20	4	8
40	8	16
60	12	24
80	16	32
100	20	40

5.5 Fault Monitoring

The ISL70321SEH has a comprehensive fault detection that actively monitors for:

- SEQUENCE ORDER FAULT - Out of sequence order
- BROWN OUT FAULT- Any VMx drops below its threshold when a sequence down is not happening
- PGOOD FAULT - VMx remains below its threshold after its ENX is released and the PGOOD timer duration has passed
- INPUT FAULT - Any VMx is high before its ENx is released
- OUTPUT FAULT - DONE remains low after the DONE was released and the PGOOD timer duration has passed
- EXTERNALLY TRIGGERED FAULTS

A fault is held in logic as a SR latch and will only reset after all VMx and UP inputs are pulled low,

When a fault is initiated, the $\overline{KILL}$ pin and all the EN_X outputs are pulled to GND simultaneously, shutting off all the power supplies by pulling all 4 ENx output down.
Externally pulling $\overline{KILL}$ below 800mV will simultaneously shut down all ENx outputs.

5.5.1 Power-Up and Power-Down Sequence Faults

During sequence up and down, the ISL70321SEH and ISL73321SEH state machine logic keeps track of which supply should be on or off and the sequence order. If during sequence up a supply indicates a high when it should be low, a fault condition is detected. Inversely, during power-down if a supply indicates a low when it should be high, a fault condition is detected unless the low is for the supply to be next low.

5.5.2 Brownout Conditions onVMx

After a completed power-up sequence, the ISL70321SEH and ISL73321SEH actively monitor the VMx pins for brownout conditions on the output of the power supplies. If any of the voltages on the VMx pins fall below the turn-off threshold (V_{OFF}), a fault is detected.

5.5.3 PGOOD Timeout Fault

If ISL70321SEH and ISL73321SEH are programmed with a PGOOD timeout period, a fault will be detected if the power supply does not reach its turn-on threshold within the alloted time.

5.5.4 Input Faults

Any incorrect state on the VMx, UP, or INIT input pins for longer than the internal filter time.

5.5.5 Externally Triggered Faults

Besides a fault indicator, the $\overline{\text{KILL}}$ pin also serves as an input pin to allow externally triggered faults and a simultaneous shut down of the sequenced power supplies. $\overline{\text{KILL}}$ is a TTL/CMOS compatible active low input. To command an external fault, the system must hold this pin below 800mV for 2µs. Typical propagation delay from $\overline{\text{KILL}}$ low to all EN pulled low is ~600ns.

5.5.6 Fault Clearing

To clear a fault condition on ISL70321SEH and ISL73321SEH, the following conditions must all be met:

- The UP pin must be below 600mV.
- All VM_X pins must be below 600mV.
- If an external fault condition was initiated, the $\overline{\text{KILL}}$ pin must be released.

5.6 Connecting Unused Rails

The simplified schematic in Figure 31 highlights the necessary connections for unused EN_X and VM_{Xun} pins. The unused VM_X and EN_X must be shorted together in pairs and each pair pulled up to VCC5 with an external resistor. An unused ENx / VMx pair can be used to establish a delayed active high output for down stream signaling.

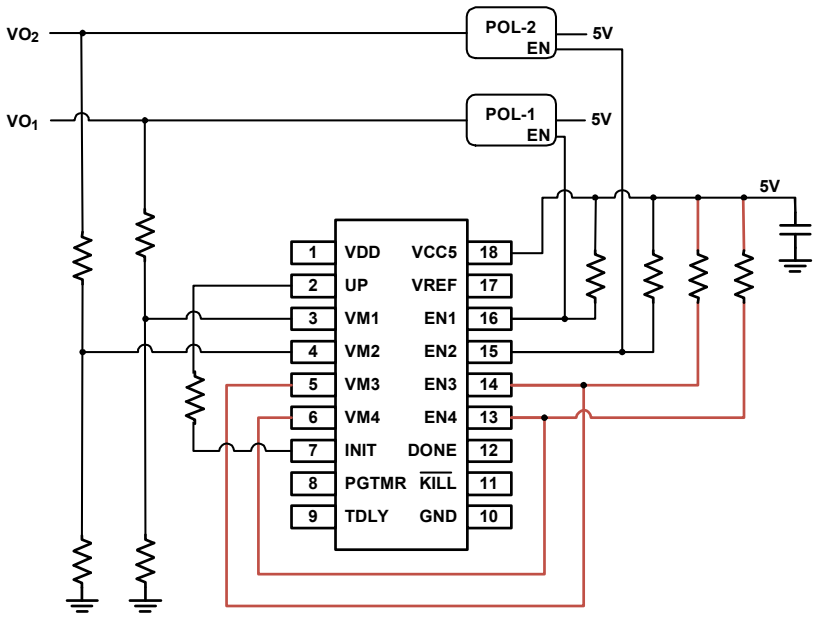


Figure 31. Connecting Unused Rails

5.7 Cascading Multiple ISL70321SEHs or ISL73321SEHs

Virtually an unlimited number of the ISL70321SEH or ISL73321SEH devices can be cascaded together to sequence an infinite number of power supplies. Figure 32 is an example of the necessary connections to sequence

eight power supplies. To sequence more power supplies, use the 12 power supply application circuit in Figure 33 and add more ISL70321SEHs or ISL73321SEHs in the middle.

Notice the first IC in the chain has its INIT pin resistively tied to its UP pin. The following devices have their INIT pins driven by the DONE pin of the preceding device. The last device in the sequence must have its DONE pin pulled high through an external resistor. Any device that is not the last in the sequence must have its DONE pin connected directly to the INIT pin of the device that is next in the sequence. All the $\overline{\text{KILL}}$ pins should be connected together and pulled high through a single external resistor.

All the VDD pins of the ISL70321SEHs or ISL73321SEHs in the cascaded chain must be connected to the same power supply. All the GND pins should be connected to the same ground point to minimize ground potential differences between ICs. Minimize trace length to the ground connection, ideally a via close to the pin should be used to connect to system ground.

The UP, INIT, and DONE pins are used for communication between the cascaded devices. Keep parasitic capacitance on these nodes to 100pF maximum. Use the ground plane to shield these traces on either side. See Figures 28 and 29 for the handshake signals in the dual and triple cascaded configurations.

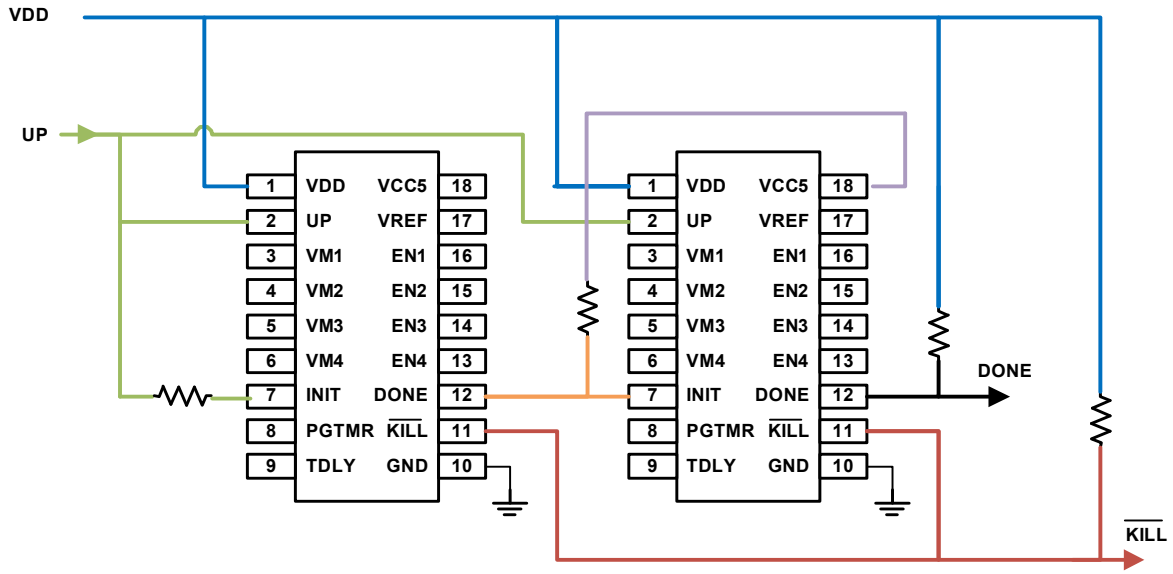


Figure 32. Sequencing Eight Power Supplies Using Two ISL70321SEHs

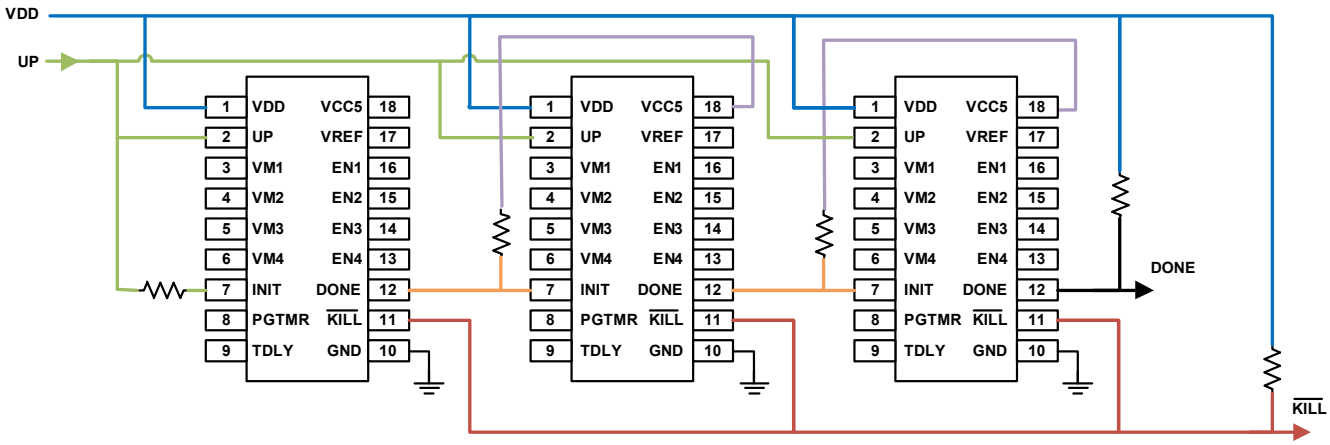


Figure 33. Sequencing Twelve Power Supplies Using Three ISL70321SEHs

5.8 Additional Information

Section intentionally left blank to amend this datasheet during the product development process.

6. Die and Assembly Characteristics

Table 3. Die and Assembly Related Information

Die Information	
Dimensions	3300µm x 6600µm (130 mils x 260 mils) Thickness: 483µm ± 25.4µm (19 mils ± 1mil)
Interface Materials	
Glassivation	Type: Silicon Oxide and Silicon Nitride Thickness: 0.3µm ± 0.03µm to 1.2µm ± 0.12µm
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 2.7µm ±0.4µm
Backside Finish	Silicon
Process	0.6µM BiCMOS Junction Isolated
Assembly Information	
Substrate Potential	GND
Additional Information	
Worst Case Current Density	$<2 \times 10^5$ A/cm_2
Transistor Count	4003
Weight of Packaged Device	0.79 grams (typical) - K18.B Package
Lid Characteristics	Finish: Gold Lid Potential: GND

6.1 Metallization Mask Layout

ISL70321SEH

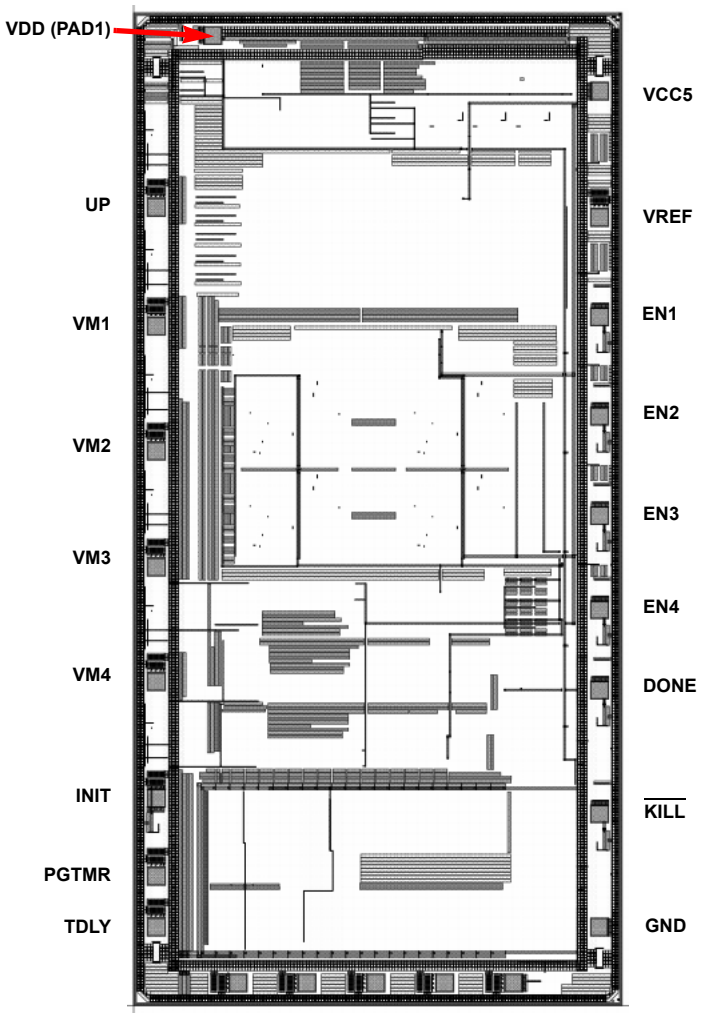


Table 4. Layout X-Y Coordinates (Centroid of bond pad)

Pad Name	Pad Number	X (µm)	Y (µm)	dX (µm)	dY (µm)	Bond Wires Size (0.001”)
VDD	1	0	0	110	110	1.25
UP	2	-368	-1123.4	110	110	1.25
VM1	3	-368	-1900.8	110	110	1.25
VM2	4	-368	-2717.95	110	110	1.25
VM3	5	-368	-3476.25	110	110	1.25
VM4	6	-368	-4225.43	110	110	1.25
INIT	7	-368	-4987.95	110	110	1.25
PGTMR	8	-368	-5497.85	110	110	1.25
TDLY	9	-368	-5830	110	110	1.25
GND	10	2526	-5830	110	110	1.25
KILL	11	2526	-5088.8	110	110	1.25
DONE	12	2526	-4279.45	110	110	1.25
EN4	13	2526	-3754.45	110	110	1.25
EN3	14	2526	-3138.8	110	110	1.25
EN2	15	2526	-2488.8	110	110	1.25
EN1	16	2526	-1838.8	110	110	1.25
VREF	17	2526	-1188.8	110	110	1.25
VCC5	18	2526	-364	110	110	1.25

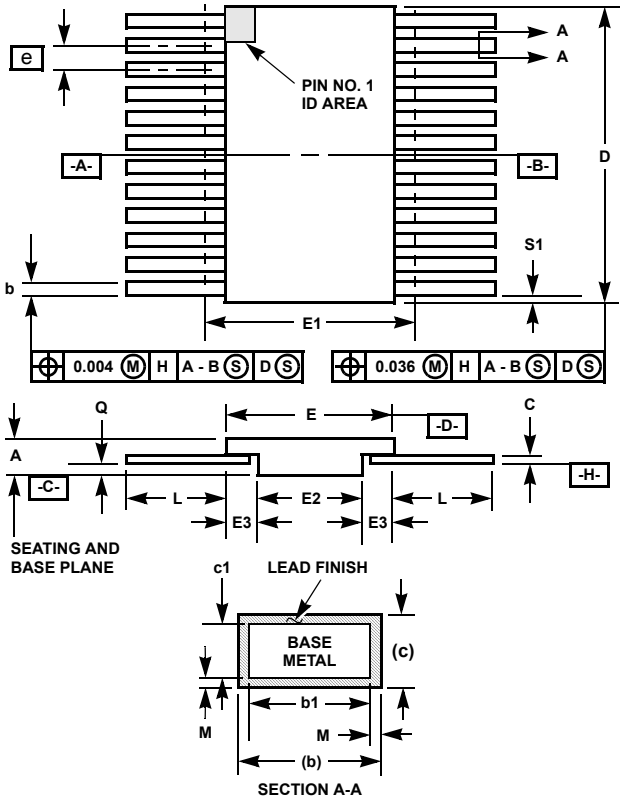
7. Revision History

Rev.	Date	Description
2.00	Nov 7, 2017	Updated Absolute Maximum Ratings section to clarify VDD, ENx, $\overline{\text{KILL}}$, and DONE.
1.00	Nov 6, 2017	Updated evaluation board part numbers to correct information. Updated ESD Circuit number for Pin 2 and Pin 18 in the pin description table.
0.00	Aug 23, 2017	Initial release

8. Package Outline Drawing

For the most recent package outline drawing, see K18.B.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K18.B
18 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	0.430	0.450	10.92	11.43	3
E	0.320	0.340	8.13	8.64	-
E1	-	0.360	-	9.14	3
E2	0.220	0.240	5.59	6.10	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.280	0.320	7.11	8.13	-
Q	0.026	0.045	0.66	1.14	8
S1	0.000	-	0.00	-	-
M	-	0.0015	-	0.04	-
N	18		18		-

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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9. About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit: www.intersil.com/glossary.

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