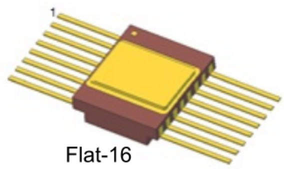
RHFAD128

Datasheet

Rad-hard, 8-channel, 50 ksps to 1 Msps, 12-bit A/D converter



Flat-16

Product status link
RHFAD128

Features

- 50 ksps to 1 Msps conversion rate
- 8-to-1-channel single input MUX
- 4-to-1-channel differential input MUX
- 3.3 V operating supply
- Independent analog and digital supplies
- Pure CMOS
- Very low consumption
- SPI, serial digital output
- Power-down function
- 300 krad TID targeted
- 125 MeV.cm²/mg SEL free

Applications

- Analog multiplexing and conversion in space and harsh environments
- Telemetry
- Housekeeping

Description

The RHFAD128 is specifically designed to sustain ionizing dose and heavy-ions for space applications by using a high-end proven CMOS technology.

This device is a low-power, multiplexed eight-channel 12-bit analog-to-digital converter for conversion from 50 ksps to 1 Msps. The architecture is based on the successive-approximation register with internal track-and-hold. The RHFAD128 features 8-single ended inputs that can be used as 4 differential inputs. The output serial data is straight binary and is compatible with SPI™.

The analog and digital power supplies operate from 2.7 V to 3.6 V, drawing a current consumption of 2 mA max. only.

The RHFAD128 is in hermetic ceramic Flat-16 leads, and works from -55 °C to + 125 °C ambient temperature.

1 Functional description

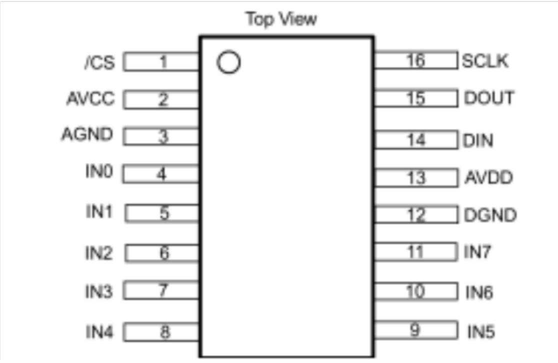


Figure 1. Pin description

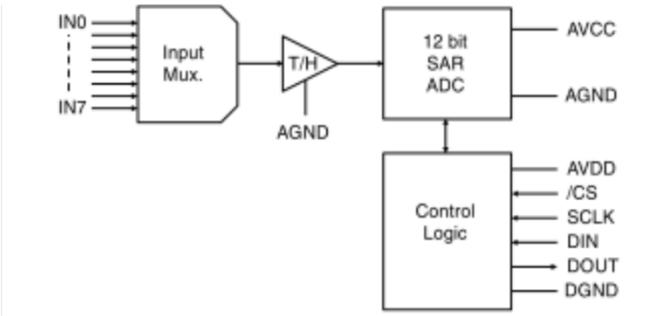


Figure 2. Block diagram

Table 1. Control register bits

Bit#	7 (MSB)	6	5	4	3	2	1	0
Symbol	DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

Table 2. Control register bit description

Bit#	Symbol	Description
7, 6, 2, 1, 0	DONTC	Do not care
5	ADD2	They determine which input channel is converted, as per Table 3. Single input channel description.
4	ADD1	
3	ADD0	

Table 3. Single input channel description

ADD2	ADD1	ADD0	Input channel
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

Table 4. Differential input channel description

ADD1	ADD0	Differential channel
0	0	IN1-IN2
0	1	IN3-IN4
1	0	IN5-IN6
1	1	IN7-IN8

1.1 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operations under these conditions is not implied.

Table 5. Absolute maximum ratings

Symbol	Parameters	Value	Unit
AVCC [1]	Maximum analog power supply between AVCC and AGND	-0.3 V to 4.8 V	V
DVCC[1]	Maximum digital power supply between DVCC and DGND	-0.3 V to AVCC+0.3 V (4.8 V max.)	V
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C
R_{thja}	Junction-to-ambient thermal resistance (Flat-16 package)[2]	120	°C/W
R_{thjc}	Junction-to-case thermal resistance (Flat-16 package) [2]	22	°C/W
V_i	Max. voltage on any pin vs. GND	-0.3 V to AVCC+0.3 V	V
I_i	Max. input current at any pin	±10	mA
ESD	HBM on all pins (human body model)	4 k	V

1. *All voltages, except differential I/O bus voltage, refer to the network ground level.*
2. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

Table 6. Operating conditions

Symbol	Parameters	Min.	Max.	Unit
AVCC	Analog supply voltage	2.7	3.6	V
DVCC	Digital supply voltage	AVCC - 0.15	AVCC + 0.15	V
VIN	Analog input voltage in single-ended	0	AVCC	V
	Analog input voltage in differential configuration, and VICM=AVCC/2 (see Figure 7. True-differential input range)	-AVCC	AVCC	
VICM	Common mode in differential configuration	0	AVCC	V
VIND	Digital input voltage	0	AVCC	V
SCLK	Clock frequency	0.1	16	MHz
T_a	Ambient temperature range	-55	+125	°C

1.2 Electrical characteristics

AVCC = DVCC = +3.3 V, sngle-ended input, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 ksps to 1 Msps, CL = 50 pF, typ. values at +25 °C, min./max. values at -55 °C/125 °C, unless otherwise specified.

Table 7. Electrical characteristics in single-ended input

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Static characteristics						
	Resolution without missing codes				12	Bits
INL	Integral non-linearity (end-point method)		−1.1	±0.6	1.1	LSB
DNL	Differential non-linearity		-0.9	±0.5	0.9	LSB
OE	Offset error		−2.3	0.8	2.3	LSB
OEM	Offset error match		−2	±0.1	2	LSB
FSE	Full scale error		−2	0.8	2	LSB
FSEM	Full scale error match		−2		2	LSB
Dynamic characteristics						
FPBW	Full power bandwidth-3 dB			6.8		MHz
SINAD	Signal-to-noise plus distortion ratio (0 to Fs/2)	FIN = 40.2 kHz, −0.02 dBFS	68	72		dB
SNR	Signal-to-noise ratio (0 to Fs/2)		69	71		dB
THD	Total harmonic distortion			−80	−74	dB
SFDR	Spurious-free dynamic range (0 to Fs/2)		75	81		dB
ENOB	Effective number of bits		11.1	11.4		Bits
ISO	Channel-to-channel isolation	FIN = 20 kHz, −0.02 dBFS	80	84		dB
IM2	2nd order intermodulation	f_a = 19.5 kHz, f_b = 20.5 kHz VINA=VINB=-6.02 dBFS		−90	−78	dB
IM3	3rd order intermodulation			−90	−72	dB
Analog input characteristics						
IDCL	DC leakage current		-1		1	µA
CINA	Input capacitance	Track mode		45		pF
		Hold mode		4.5		pF
Digital input characteristics						
VIH	Input high voltage		2.1			V
VIL	Input low voltage				0.8	V
IIN	Digital input current	VIN = 0 V or DVCC	-1		1	µA
CIND	Digital input capacitance			3.5		pF
Digital output characteristics, output coding: straight (natural) binary						
VOH	Output high voltage	I_{source}=1 mA	2.8			V
VOL	Output low voltage	I_{sink}=1 mA			0.4	V

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
IOZH, IOZL	Hi-impedance output leakage current		-1		1	μA
COUT	Hi impedance output capacitance			3.5		pF
Power supply characteristics, CL=10 pF						
IAVCC + IDVCC	Total supply current, normal mode (CS low)	AVCC = DVCC = +2.7 V to +3.6 V, f_S=1 MSPS, FIN=40 kHz		1.65	2	mA
	Total supply current, shutdown mode (CS high)	AVCC = DVCC = +2.7 V to +3.6 V, f_S=0		2	10	μA
AC characteristics (AVCC = DVCC = +2.7 V to +3.6 V)						
$t_{CONVERT}$	Conversion (hold) time			13		SCLK cycles
DC	SCLK duty cycle		40		60	%
t_{ACQ}	Acquisition (track) time cycles	See Figure 5. Serial timing diagram		3		SCLK cycles
	Throughput time Acquisition time + Conversion time			16		SCLK cycles
t_{AD}	Aperture delay			4		ns
Timing specifications (AVCC = DVCC = +2.7 V to +3.6 V) (1)						
t_{CSH}	CS/ hold time after SCLK rising edge	(2)	10	0		ns
t_{CSS}	CS/ setup time prior SCLK rising edge	(2)	10	4.5		ns
t_{EN}	CS/ falling edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT access time after SCLK falling edge			17	27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		7			ns
t_{DS}	DIN setup time prior to SCLK rising edge		10			ns
t_{DH}	DIN hold time after SCLK rising edge		10			ns
t_{DIS}	CS/ rising edge to DOUT high-impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	ns
t_{CH}	Min. SCLK high time			0.4 x t_{SCLK}		ns
t_{CL}	Min. SCLK low time			0.4 x t_{SCLK}		ns

1. *Limits are guaranteed by functional test.*
2. *Clock may be in any state (high or low) when CS/ goes high. Set-up and hold time restrictions apply to CS/ going low only.*

AVCC = DVCC = +3.3 V, differential input (see figure 4 for configuration), AGND = DGND = 0 V, f_{SCLK} = 16 MHz, f_{SAMPLE} = 1 Msps, CL = 50 pF, typ. values at +25 °C, min./max. values at -55 °C/125 °C, unless otherwise specified.

Table 8. Electrical characteristics in differential input

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Static characteristics						
INL	Integral non-linearity (end point method)	VICM=AVCC/2	-0.9	±0.3	0.9	LSB
DNL	Differential non-linearity		−0.8	±0.3	0.8	LSB
OE	Offset error	VICM=AVCC/2 for all	−1.5	0.2	1.5	LSB
OEM	Offset error match		−1.5	±0.3	1.5	LSB
FSE	Full scale error		−2	0.5	2	LSB
FSEM	Full scale error match		−2		2	LSB
Dynamic characteristics						
SINAD	Signal-to-noise plus distortion ratio (0 to Fs/2)	FIN=40.2 kHz, −0.02 dBFS	69.3	72		dB
SNR	Signal-to-noise ratio (0 to Fs/2)		71	73		dB
THD	Total harmonic distortion			−80	−74	dB
SFDR	Spurious-free dynamic range (0 to Fs/2)		75	81		dB
ENOB	Effective number of bits		11.2	11.6		Bits
ISO	Channel-to-channel isolation	FIN=20 kHz, −0.02 dBFS	85	95		dB
IM2	2nd order intermodulation	f_a = 19.5 kHz, f_b=20.5 kHz VINA=VINB=-6.02 dBFS		−90	−78	dB
IM3	3rd order intermodulation	f_a = 19.5 kHz, f_b=20.5 kHz VINA=VINB=- 6.02 dBFS		−90	−72	dB

1.3 Radiations

Total dose (MIL-STD-883 TM 1019):

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFAD128 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All provided parameters in Table 7. Electrical characteristics in single-ended input apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID)
- The initial characterization is performed in qualification only on both biased and unbiased parts
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification

Heavy-ions:

The behavior of the product when submitted to heavy-ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 9. Radiations

Type	Characteristics	Value	Unit
TID	High dose rate (50 - 300 rad/s) up to	300	krad
Heavy-ions	SEL immune up to (with a particle angle of 60 ° at 125 °C)	125	MeV.cm²/mg
	SEL immune up to (with a particle angle of 0 ° at 125 °C)	62	
	SEU immune up to (at 25 °C)	32	

1.4 Timing diagrams

Figure 3. Operational timing diagram in single-ended input

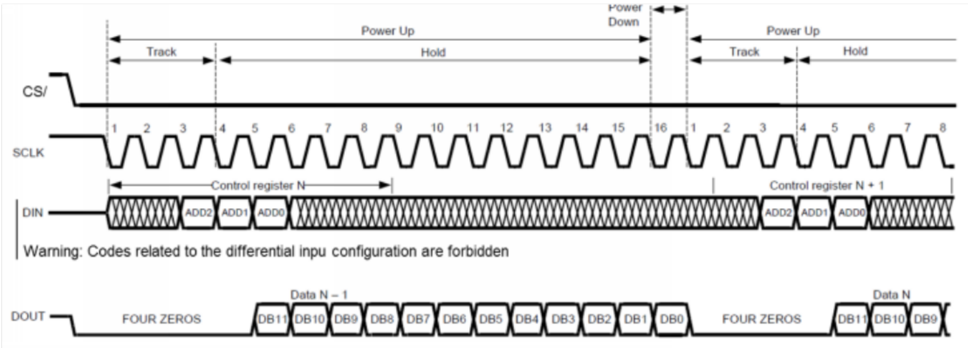


Figure 4. Operational timing diagram in differential input

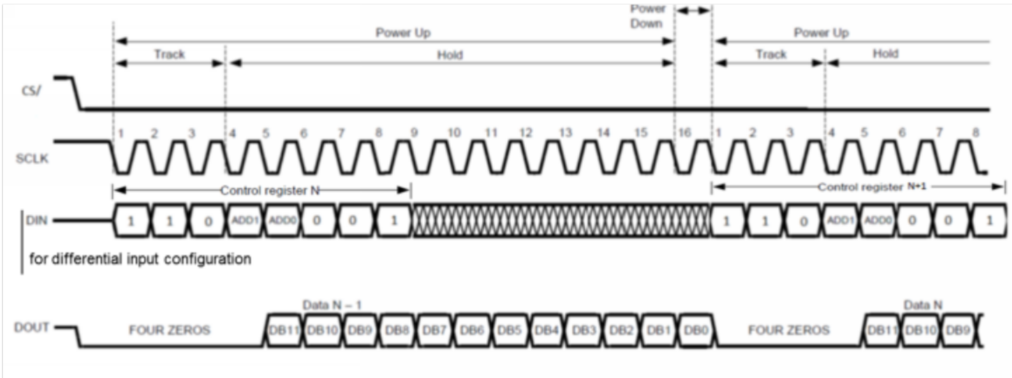
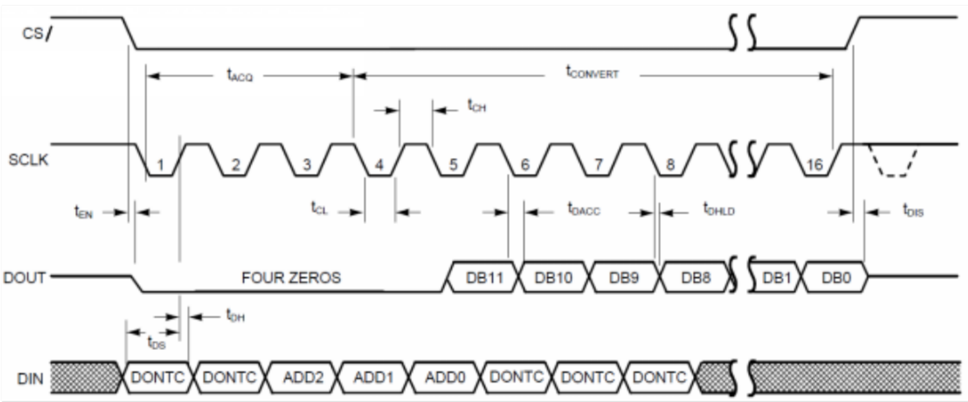


Figure 5. Serial timing diagram



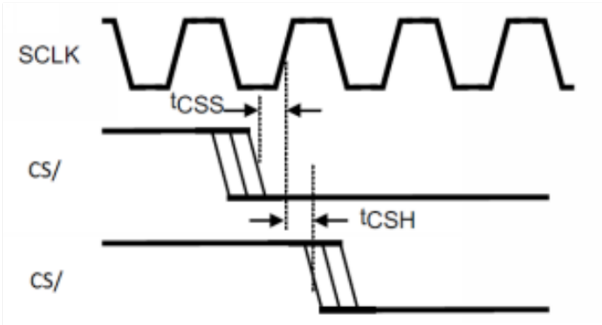
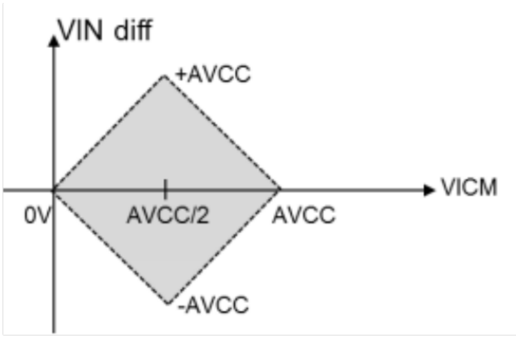


Figure 6. SCLK and CS/ timings

1.5 Differential input

Figure 7. **True-differential input range**



The maximum differential input swing is limited by the input common mode value (VICM) and it is limited by the grey area as shown in Figure 7. True-differential input range. The maximum value equals to +/-AVCC for VICM=AVCC/2.

1.6 Definitions

- **Acquisition time** is the time required to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage
- **Aperture delay** is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion
- **Channel-to-channel isolation** is the residual noise injected on the selected channel by other unselected channels
- **Conversion time** is the time required, after the input voltage is acquired, to convert the input voltage to a digital word
- **Differential non-linearity (DNL)** is the maximum deviation from the ideal step size of 1 LSB
- **Duty cycle** is the ratio, for a periodic digital signal, of the high level duration divided by the total period
- **Effective number of bits (ENOB)** is a method to specify signal-to-noise and distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits
- **Full power bandwidth** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input
- **Full scale error (single-ended input)** is the deviation of the last code transition (111...110) to (111...111) from the ideal (AVCC -1LSB), after adjusting for offset error
- **Positive full scale error (differential input)** is the deviation of the last code transition (111...110) to (111...111) from the ideal (AVCC -1LSB), after adjusting for offset error
- **Negative full scale error (differential input)** is the deviation of the last code transition (111...110) to (111...111) from the ideal (-AVCC +1LSB), after adjusting for offset error
- **Integral non-linearity (INL)** is the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value
- **Intermodulation distortion (IMD)** is the result of the product of two pure sine waves at frequency f_a and f_b applied to the ADC input. To avoid clipping when the sine waves are in phase, the level must be just below -6 dBFS. Assuming that the level of the two tones is equal, IMD2 is the difference in dBc between level (f_a or f_b) and level($f_a \pm f_b$). IMD3 is is the difference in dBc between level (f_a or f_b) and level ($2f_a \pm f_b$) or level ($f_a \pm 2f_b$)
- **Missing codes** are those output codes that never appear on the ADC outputs. The RHFAD128 is guaranteed not to have any missing codes
- **Offset error (single-ended input)** is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND +1 LSB)
- **Signal-to-noise ratio (SNR)** is the ratio, expressed in dB, of the RMS value of the fundamental of input signal to the RMS value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC-component
- **Signal-to-noise plus distortion (S/N+D or SINAD)** is the ratio of the RMS value of the fundamental of input signal to the RMS value of all of the other spectral components below half the sampling frequency, including harmonics but excluding DC-component
- **Spurious free dynamic range (SFDR)** is the difference, expressed in dB, between the desired signal amplitude of fundamental to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present on the input and may or may not be a harmonic
- **Total harmonic distortion (THD)** is the ratio, expressed in dBc, of the RMS total of the first nine harmonic components on the output to the RMS level of fundamental of the input signal frequency as seen on the output. THD is calculated as $THD=20\log10[\mathrm{sqrt}((Af2^2+\ldots+Af10^2)/Af1^2)]$ where Af1 is the RMS power of the fundamental on the output and Af2 to Af10 are the RMS power in the first nine harmonic frequencies
- **Throughput time** is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion time

1.7 PCB layout precautions

- A ground plane on each layer of the PCB with multiple vias dedicated to interconnection is recommended for high speed circuit applications to provide low parasitic inductance and resistance. The goal is to have a “common ground plane” where AGND and DGND are connected with the lowest DC resistance and lowest AC impedance
- The separation of the analog signal from the digital output is mandatory to prevent noise from coupling onto the input signal
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high frequency bypassing and reduce harmonic distortion
- All leads must be as short as possible, especially for the analog input, so to decrease parasitic capacitance and inductance
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest possible routing tracks. One way to reduce capacitive load is to remove the ground plane under the output digital pins and layers at high sampling frequencies
- Choose the smallest possible component sizes (SMD)

2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 Flat-16 package information

The upper metallic lid is electrically connected to AGND and DGND.

Figure 8. Flat-16 package information outline

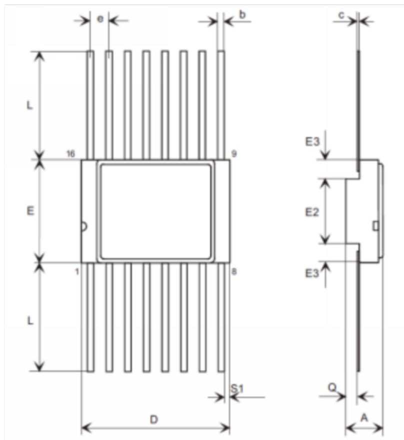


Table 10. Flat-16 package mechanical data

Ref.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	0.091		0.107
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.75		10.13	0.384		0.399
E	6.75		7.06	0.266		0.278
E2		4.32			0.170	
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

3 Ordering information

Table 11. Order code

Order code	SMD(1)	Quality level	Temp. range	Mass	Package	Marking(2)	Packing
RH-AD128K1	-	Engineering model	-55 °C to +125 °C	0.65 g	Flat-16	RHFAD128K1	Strip pack
RHFAD128K01V(3)	TBD	QML-V Flight				TBD	

1. *Standard microcircuit drawing.*
2. • *Specific marking only. Complete marking includes the following:*
   • *ST logo*
   • *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   • *Country of origin (FR = France).*
3. *QML-V qualification and SMD are being got.*

4 Other information

Date code:

The date code is structured as follows:

Engineering model: EM xyywwz

where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Note: Please, contact ST for details on the documentation of other quality levels

Table 12. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to the TN1181 on engineering models ST Rennes assembly lot ID

Quality level	Item
QML-V Flight	Certificate of conformance including Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Pre-cap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
12-Mar-2018	1	Initial version.

Contents

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